

WAGO → I/O → SYSTEM 750

**Fieldbus Independent
I/O Modules**

**Incremental Encoder Interfaces
750-631, (/xxx-xxx)**



Manual

Version 1.1.0

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Every conceivable measure has been taken to ensure the correctness and completeness of this documentation. However, as errors can never be fully excluded, we would appreciate any information or ideas at any time.

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We wish to point out that the software and hardware terms as well as the trademarks of companies used and/or mentioned in the present manual are generally trademark or patent protected.

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1 Important Comments

To ensure fast installation and start-up of the units described in this manual, we strongly recommend that the following information and explanations are carefully read and abided by.

1.1 Legal Principles

1.1.1 Copyright

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1.1.2 Personnel Qualification

The use of the product detailed in this manual is exclusively geared to specialists having qualifications in PLC programming, electrical specialists or persons instructed by electrical specialists who are also familiar with the valid standards. WAGO Kontakttechnik GmbH & Co. KG declines all liability resulting from improper action and damage to WAGO products and third party products due to non-observance of the information contained in this manual.

1.1.3 Intended Use

For each individual application, the components supplied are to work with a dedicated hardware and software configuration. Modifications are only permitted within the framework of the possibilities documented in the manuals. All other changes to the hardware and/or software and the non-conforming use of the components entail the exclusion of liability on part of WAGO Kontakttechnik GmbH & Co. KG.

Please direct any requirements pertaining to a modified and/or new hardware or software configuration directly to WAGO Kontakttechnik GmbH & Co. KG.

1.2 Symbols



Danger

Always abide by this information to protect persons from injury.



Warning

Always abide by this information to prevent damage to the device.



Attention

Marginal conditions must always be observed to ensure smooth operation.



ESD (Electrostatic Discharge)

Warning of damage to the components by electrostatic discharge. Observe the precautionary measure for handling components at risk.



Note

Routines or advice for efficient use of the device and software optimization.



More information

References on additional literature, manuals, data sheets and INTERNET pages

1.3 Number Notation

Number Code	Example	Note
Decimal	100	normal notation
Hexadecimal	0x64	C notation
Binary	'100' '0110.0100'	Within ' Nibble separated with dots

1.4 Safety Notes



Warning

Switch off the system prior to working on bus modules!

In the event of deformed contacts, the module in question is to be replaced, as its functionality can no longer be ensured on a long-term basis.

The components are not resistant against materials having seeping and insulating properties. Belonging to this group of materials is: e.g. aerosols, silicones, triglycerides (found in some hand creams).

If it cannot be ruled out that these materials appear in the component environment, then additional measures are to be taken:

- installation of the components into an appropriate enclosure
 - handling of the components only with clean tools and materials.
-



Attention

Cleaning of soiled contacts may only be done with ethyl alcohol and leather cloths. Thereby, the ESD information is to be regarded.

Do not use any contact spray. The spray may impair the functioning of the contact area.

The WAGO-I/O-SYSTEM 750 and its components are an open system. It must only be assembled in housings, cabinets or in electrical operation rooms. Access must only be given via a key or tool to authorized qualified personnel.

The relevant valid and applicable standards and guidelines concerning the installation of switch boxes are to be observed.



ESD (Electrostatic Discharge)

The modules are equipped with electronic components that may be destroyed by electrostatic discharge. When handling the modules, ensure that the environment (persons, workplace and packing) is well grounded. Avoid touching conductive components, e.g. gold contacts.

1.5 Scope

This manual describes the Digital Input Module **750-631 Incremental Encoder Interface** of the modular WAGO-I/O-SYSTEM 750.

Handling, assembly and start-up are described in the manual of the Fieldbus Coupler. Therefore this documentation is valid only in the connection with the appropriate manual.

2 I/O Modules

2.1 Special Modules

2.1.1 Overview Incremental Encoder Interfaces 750-631, (/xxx-xxx)

I/O module	750-631	750-631/ 000-001	750-631/ 000-004	750-631/ 000-010	750-631/ 000-011
Function	Incremental encoder interface	Incremental encoder interface, single report	Incremental encoder interface, RS422	Incremental encoder interface	Incremental encoder interface, single report
Sensor input	differential	differential	differential	single ended, differential	single ended, differential
Digital input	Latch, gate	Latch, gate	Latch, gate, ext. error	Latch, gate, ext. error	Latch, gate, ext. error
sensor supply voltage	DC 5 V	DC 5 V	DC 5 V (RS422)	DC 5 V ... 24 V	DC 5 V ... 24 V
Report	4-fold	single	4-fold	4-fold	single
Data width	32 bit	32 bit	32 bit	32 bit	32 bit
Remark	No longer available	No longer available			

2.1.2 750-631(750-631/000-001) [Incremental Encoder Interface]

2.1.2.1 Variations

Item-No.	Designation	Description
750-631	Increment.Enc.	Incremental Encoder Interface, 4-fold report
750-631/000-001	Increment.Enc./single report	Incremental Encoder Interface, single report

2.1.2.2 View

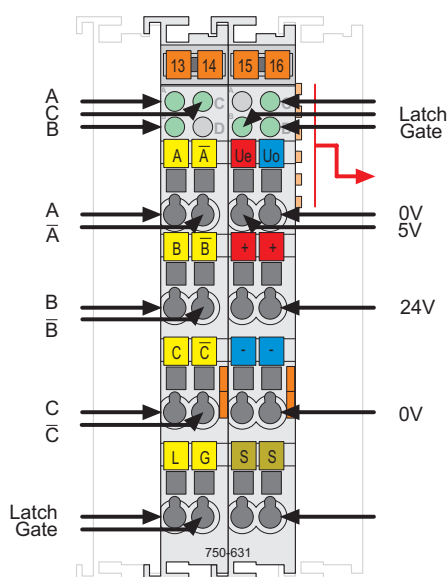


Fig. 2.1.2-2: Incremental Encoder Interface 750-631

g063100e

2.1.2.3 Description

This module is an interface for the connection of any incremental encoder.

The transmitter can be directly supplied from the Ue and U0 terminations of the module.

The shield (screen) is directly connected to the carrier rail.

A 16 bit counter with quadrature encoder interface as well as a 16 bit latch for the zero impulse can be read, set, or enabled. The count of the counter will be transmitted fast and interference-free over the fieldbus to the PC, PLC, or NC. A counter lock-out is possible using input Gate.

Individual green status LEDs indicate the operating status of the module and the signal status of the A, B and C as well as latch and gate inputs.

Any configuration of the specialty modules is possible when designing the fieldbus node. Grouping of module types is not necessary.



Attention

This module has no power contacts. For field supply to downstream I/O modules, a supply module will be needed.

The module 750-631 and its variations can be used with all couplers/controllers of the WAGO-I/O-SYSTEM 750 (except for the economy types 750-320, -323, -324 and -327).

This description is valid for the XXXX2B1A... and XXXX2B1B... hardware and software versions. The version is specified in the manufacturing number, which is part of the lateral marking on the module.

2.1.2.4 Display Elements

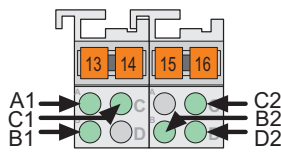


Fig. 2.1.2-2: Display Elements
 g063102x

LED	Channel	State	Function
A1 green	A	off	Signal (0)
		on	Signal (1)
B1 green	B	off	Signal (0)
		on	Signal (1)
C1 green	C	off	Signal (0)
		on	Signal (1)
B2 green	Latch	off	Signal (0)
		on	Signal (1)
C2 green	Function	off	No operational readiness or the internal data bus communication is interrupted
		on	Operational readiness and trouble-free internal data bus communication
D2 green	Gate	off	Signal (0)
		on	Signal (1)

2.1.2.5 Schematic Diagram

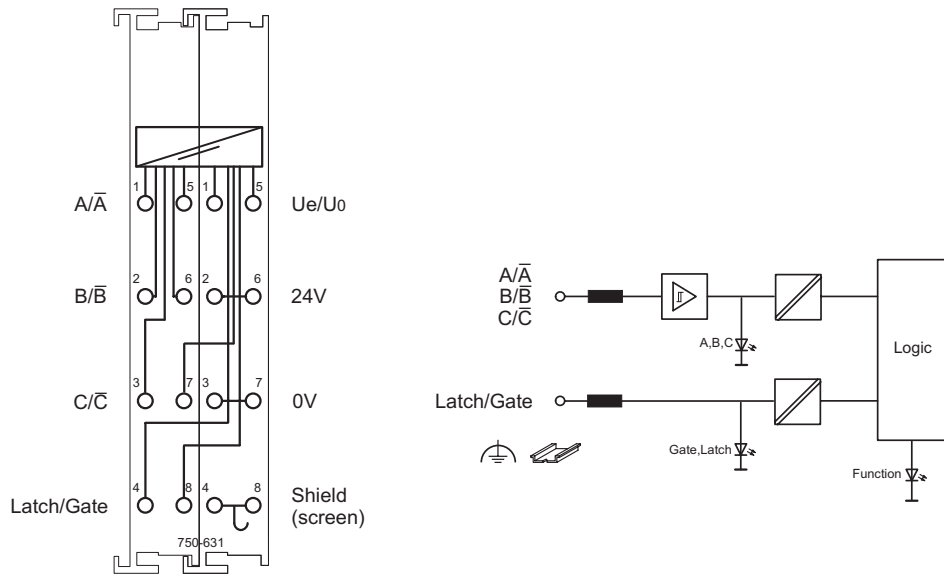






Fig. 2.1.2-1: Incremental Encoder Interface 750-631

g063101e

2.1.2.6 Technical Data

Module Specific Data		
Sensor connection	A, /A, B, /B, C, /C (/A, /B, /C are inversed)	
Current consumption (internal)	25 mA	
Signal voltage A, B, C, /A, /B, /C	(0) $U \leq 2.0 \text{ V}$ (1) $U \geq 5.0 \text{ V}$	
Signal voltage Latch, Gate	(0) $U \leq 2.0 \text{ V}$ (1) $U \geq 11.0 \text{ V}$	
Sensor power supply	DC 5 V	
Sensor output current _{max.}	200 mA	
Counter	16 bits binary	
Operating frequency	470 kHz	
Quadrature decoder	4-fold report (750-631), single report (750-631/000-001)	
Zero impulse latch	16 bits	
Commands	read, set, enable	
Voltage supply	DC 24 V (-15 % ... +20 %)	
Current consumption _{typ.}	6 mA without sensor	
Internal bit width	1 x 32 bits 1 x 8 bits control/status 1 x 8 bits reserved	
Isolation	500 V (System/Supply)	
Dimensions W x H* x L * from upper edge of 35 DIN rail	24 mm x 64 mm x 100 mm	
Weight	ca. 105 g	
Approvals (cf. Chapter 2.2 of the Coupler/Controller Manual)		
	cUL _{US} (UL508)	
	cUL _{US} (UL1604)	Class I Div2 ABCD T4A
	KEMA	II 3 G EEx nA II T4
	Conformity Marking	



More Information

Detailed references to the approvals are listed in the document "Overview Approvals WAGO-I/O-SYSTEM 750", which you can find on the CD ROM ELECTRONICC Tools and Docs (Item-No.: 0888-0412)

or in the internet under:

www.wago.com → Documentation → WAGO-I/O-SYSTEM 750 → System Description

2.1.2.7 Functional Description

The incremental encoder interface is used to evaluate two 90° phase-shifted track signals delivered by digital encoders. If required, the signals generated by the index track can also be processed. Control via two 24 V signals is optional.

Typically, incremental encoders provide two signals of the encoder track, both 90° offset. These signals are labeled A and B. To improve the common mode rejection ratio, both signals are transmitted as differential signals. In addition to the A signal, the complement signal /A is also transmitted. The difference between the input signals is performed by the incremental encoder interface.

By exchanging A and /A the phase position will turn from A to B, thus allowing the desired counting direction to be preset via the wiring configuration.

Most incremental encoders have an index track in addition to the two track signals. This index track generates a single pulse per encoder revolution. This pulse can be used to determine the absolute encoder position within a revolution. Through the appropriate initialization, the current counter value is transmitted to a latch register using the index pulse. Since the index pulse has the same duration as a track signal, the latch process should always be performed in the same rotational direction.

The encoder is supplied with 5 V derived from the terminations Ue and U0. This voltage is generated from an external 24 V power supply. The inputs 0 V and U0 are connected internally.

The latch input controls the overtaking of the actual counter value into the latch register. This input is activated by the control bit EN_LATEXT ("1"). EN_LACT has to be deactivated ("0"). After activation, the first edge transition from 0 V to 24 V at the latch input takes the actual counter value into the latch register. The control bit EN_LATEXT must be deleted and reset, so that the counter value can be stored again.

The gate input stops the counter. Only 0 V or an open connection initialize the counter. 24 V stops the counting process.

The latch and gate inputs are 24 V.

Overview of Inputs and Outputs:

In-/Output	Type	Function
Signal A and Signal /A	Input, TTL	Incremental pulse signals for channel A
Signal B and Signal /B	Input, TTL	Incremental pulse signals for channel B
Signal C and Signal /C	Input, TTL	Track signal for the index channel of the sensor
Shield	Input	Shield connection for encoder wiring
Sensor 0 V	Output, Vers.	Ground for sensor signals and supply
Sensor +5 V	Output, Vers.	5 V supply for encoder
+24 V	Input, Vers.	24 V supply voltage for the sensor and data processing
0 V	Input, Vers.	Ground for the 24 V supply voltage, internally connected to sensor V0
Gate	Input, 24 V	24 V input for gate signal
Latch	Input, 24 V	24 V input for Latch signal

2.1.2.8 Process Image

Using the I/O module 750-631, a 6 byte input and output process image can be transferred to the fieldbus coupler / controller via one logical channel. The data sent and received is stored in 2 output bytes (D0, D1) and 4 input bytes (D0, D1, D3, D4). The output bytes D2 ... D4 and the input byte D2 are reserved and without function. One control byte (C0) and one status byte (S0) are used to control the data flow.



Attention

The representation of the process data of some I/O modules or their variations in the process image depends on the fieldbus coupler/-controller used. Please take this information as well as the particular design of the respective control/status bytes from the section "Fieldbus Specific Design of the Process Data" included in the description concerning the process image of the corresponding coupler/controller.

Input data		Output data	
S0	Status byte	C0	Control byte
D0	Counter value byte 0 (LSB)	D0	Setpoint value byte 0 (LSB)
D1	Counter value byte 1 (MSB)	D1	Setpoint value byte 1 (MSB)
D2	reserved	D2	reserved
D3	Latched value byte 0 (LSB)	D3	reserved
D4	Latched value byte 1 (MSB)	D4	reserved

Control byte C0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	CNT_ SET	EN_ LATEXT	EN_ LATC

EN_
LATC The counter is set with a rising edge of CNT_SET to the value that is specified via the process data.

EN_
LATEXT The external latch input is activated. With the first external latch pulse after validity of the EN_LATEXT bit, the counter value is stored in the latch register. The following pulses have no influence on the latch register when the bit is set.

CNT_
SET The zero point latch (C input) is activated. With the first external latch pulse after the validity of the EN_LATC bit, the counter value is stored in the latch register (this has priority over EN_LATEX). The following pulses have no influence on the latch register when the bit is set.

0 reserved

Status byte S0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	OVER- FLOW	UNDER- FLOW	CNTSET _ACK	LA- TEXT_ VAL	LATC_ VAL

LATC_VAL A zero point latch has occurred. The data D3, D4 in the process image corresponds to the latched counter value when the bit is set. To reactivate the latch input, EN_LATC must first be cancelled and then the bit must be set again.

LATEXT_
VAL An external latch pulse has occurred. The data D3, D4 in the process image corresponds to the latched counter value when the bit is set. To reactivate the latch input, EN_LATEXT must first be cancelled and then the bit must be set again.

CNTSET_
ACK The data for setting the counter has been accepted from the module.

UNDER-
FLOW This bit is set if an underflow (0 to 65535) of the 16-bit counter occurs. It is reset when the counter drops below two thirds of the measurement range (43690 to 43689) or as soon as an overflow occurs.

OVER-
FLOW This bit is set if an overflow (65535 to 0) of the 16-bit counter occurs. It is reset if the counter exceeds a third of the measurement range (21845 to 21846) or as soon as an underflow occurs.

0 reserved

The following tasks can be performed or checked via the control and status byte:

Extending the counter above 16 bits:

The internal counter has a width of 16 bits. Should the application require an extended range for the location values, the extended counter range may be calculated within the control system using the location-difference-integration method. This method uses the control system to store the last location value (counter value). Any new location value will have the previously stored counter value subtracted from it. Using the sign bit, this difference will be completed with the desired number of extension bits and then be added to the accumulated location value. It is assumed that the counter difference of the two counter queries is smaller than (16-1) bits therefore counter overflows need not be considered.

Another method calculates the counter extension separately by adding the bit OVERFLOW (status bit 4) or subtracting the bit UNDERFLOW (status bit 3) once, each time the counter value is read. Between two counter queries, the counter value should not be increased or decreased by more than $1/3 \times 0xFFFF$. Due to the separate calculation of the counter extension, this procedure allows for calculation using smaller data widths.

Setting the counter value:

Presetting the counter value is possible via the CNT_SET bit (control bit 2). The new counter value is transferred in the load value. When the CNT_SET bit is set from "0" to "1", the counter is loaded with the load value. The CNTSET_ACC bit (status bit 2) is set to "1" when the loading is completed

Maintaining the present counter value:

The present counter value may be maintained or latched via the external latch input. To do so, the EN_LATEXT bit (control bit 1) is set in the control word. Upon transition from "0" to "1", the latch value will contain the counter value at the time of the edge transition. Upon completion of the latch process the LATEXT_VAL bit (status bit 1) will be set to "1". Calculating the extended latch value is done as shown above.

Maintaining a reference point:

The storage of a present counter value may also be accomplished via the index pulse from the encoder. Releasing is done when the EN_LATC bit (control bit 0) is set to "1". The storage of the counter value is completed when LATC_VAL = 1 (status bit 0).

2.1.3 750-631/000-004 [Incremental Enc./ RS422]

Incremental Encoder Interface RS 422

2.1.3.1 View

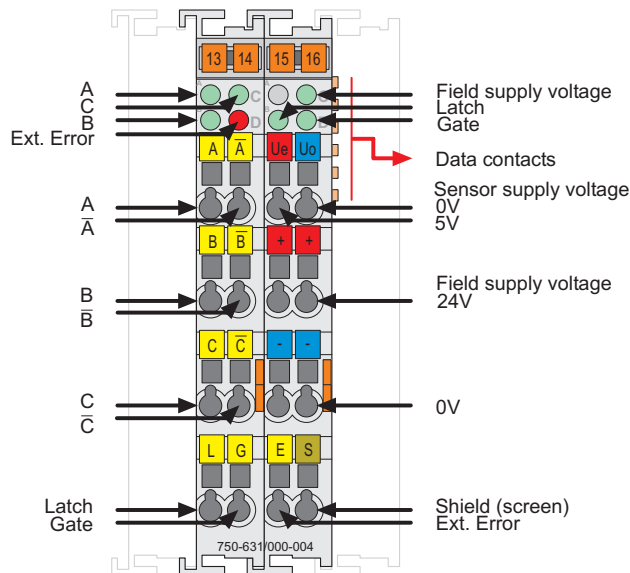


Fig. 2.1.3-1: View

g063140e

2.1.3.2 Description

This module is an interface for the connection of any incremental encoder.

The transmitter can be directly supplied from the Ue and U0 terminations of the module.

The shield (screen) is directly connected to the carrier rail.

A 16 bit counter with quadrature encoder interface as well as a 16 bit latch for the zero impulse can be read, set, or enabled. The count of the counter will be transmitted fast and interference-free over the fieldbus to the PC, PLC, or NC. A counter lock-out is possible using input Gate.

Individual green status LEDs indicate the operating status of the module and the signal status of the A, B and C as well as latch and gate inputs.

Any configuration of the specialty modules is possible when designing the fieldbus node. Grouping of module types is not necessary.



Attention

This module has no power contacts. For field supply to downstream I/O modules, a supply module will be needed.

The module 750-631 and its variations can be used with all couplers/controllers of the WAGO-I/O-SYSTEM 750 (except for the economy types 750-320, -323, -324 and -327).

This description is valid for the XXXX3E08... hardware and software versions. The version is specified in the manufacturing number, which is part of the lateral marking on the module.

2.1.3.3 Display Elements

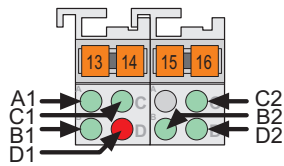


Fig. 2.1.3-2: Display Elements
 g063142x

LED	Channel	State	Function
A1 green	A	off	$U_A = 0 \text{ V}$, $U_{/A} = 5 \text{ V}$
		on	$U_A = 5 \text{ V}$, $U_{/A} = 0 \text{ V}$
B1 green	B	off	$U_B = 0 \text{ V}$, $U_{/B} = 5 \text{ V}$
		on	$U_B = 5 \text{ V}$, $U_{/B} = 0 \text{ V}$
C1 green	C	off	$U_C = 0 \text{ V}$, $U_{/C} = 5 \text{ V}$
		on	$U_C = 5 \text{ V}$, $U_{/C} = 0 \text{ V}$
D1 red	Ext. Error	off	$U \geq 5.0 \text{ V}$ or open connection
		on	$U < 0.5 \text{ V}$
B2 green	Latch	off	$U \leq 5.0 \text{ V}$
		on	$U \geq 15.0 \text{ V}$
C2 green	Field supply	off	24 V field supply voltage missing
		on	24 V field supply voltage ok
D2 green	Gate	off	$U \leq 5.0 \text{ V}$
		on	$U \geq 15.0 \text{ V}$

2.1.3.4 Schematic Diagram

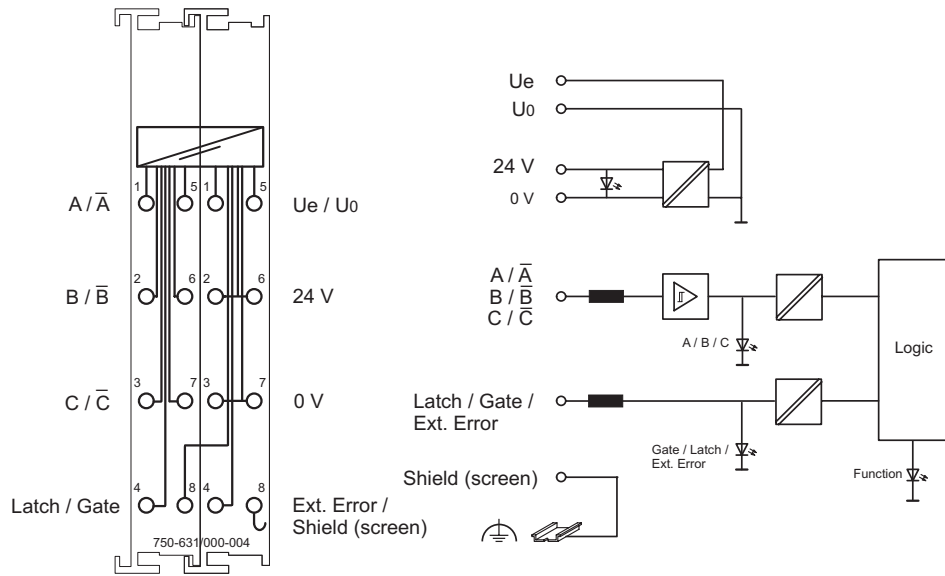






Fig. 2.1.3-2: Schematic Diagram

g063141e

2.1.3.5 Technical Data

Module Specific Data	
Sensor connection	A, /A, B, /B, C, /C (/A, /B, /C are inversed)
Signal voltage A, B, C, /A, /B, /C	(0) $U_{ABC} = 0 \text{ V}$, $U_{/A/B/C} = 5 \text{ V}$ (1) $U_{ABC} = 5 \text{ V}$, $U_{/A/B/C} = 0 \text{ V}$
Signal voltage Latch, Gate	(0) $U \leq 5.0 \text{ V}$ (1) $U \geq 15.0 \text{ V}$
Signal voltage Ext. Error	(0) $U \geq 5.0 \text{ V}$ or open connection (1) $U < 0.5 \text{ V}$
Sensor power supply	DC 5 V
Sensor output current $_{\text{max.}}$	200 mA
Counter	16 bits binary
Operating frequency	1 MHz
Quadrature decoder	4-fold report
Zero impulse latch	16 bits
Commands	read, set, enable
Voltage supply	DC 24 V (-15 % ... +20 %)
Current consumption (internal)	25 mA
Current consumption (field) $_{\text{typ.}}$	10 mA without sensor
Internal bit width	1 x 32 bits 1 x 8 bits control/status 1 x 8 bits reserved
Isolation	500 V (System/Supply)
Dimensions W x H* x L * from upper edge of 35 DIN rail	24 mm x 64 mm x 100 mm
Weight	ca. 105 g

Approvals (cf. Chapter 2.2 of the Coupler/Controller Manual)		
	cUL _{US} (UL508)	
	cUL _{US} (UL1604)	Class I Div2 ABCD T4A
	KEMA	II 3 G EEx nA II T4
	Conformity Marking	



More Information

Detailed references to the approvals are listed in the document "Overview Approvals WAGO-I/O-SYSTEM 750", which you can find on the CD ROM ELECTRONICC Tools and Docs (Item-No.: 0888-0412)

or in the internet under:

www.wago.com → Documentation → WAGO-I/O-SYSTEM 750 → System Description

2.1.3.6 Functional Description

The incremental encoder interface is used to evaluate two 90° phase-shifted track signals delivered by digital encoders. If required, the signals generated by the index track can also be processed. Control via two 24V signals is optional.

Typically, incremental encoders provide two signals of the encoder track, both 90° offset. These signals are labelled A and B. To improve the common mode rejection ratio, both signals are transmitted as differential signals. In addition to the A signal, the complement signal /A is also transmitted. The difference between the input signals is performed by the incremental encoder interface.

By exchanging A and /A the phase position will turn from A to B, thus allowing the desired counting direction to be preset via the wiring configuration.

Most incremental encoders have an index track in addition to the two track signals. This index track generates a single pulse per encoder revolution. This pulse can be used to determine the absolute encoder position within a revolution. Through the appropriate initialization, the current counter value is transmitted to a latch register using the index pulse. Since the index pulse has the same duration as a track signal, the latch process should always be performed in the same rotational direction.

If the rotary transducer is equipped with a monitoring electronics with NPN alarm output, then this output can be connected to the external error input. The input is switching negatively, i.e., 0V is logically mapped to 1.

With connector versions A and D, the 5V supply for the sensor can be tapped off at the outputs Ue and U0. This supply voltage is generated from 24V to be provided externally. The inputs 0V and U0 are connected internally.

The latch input controls the overtaking of the actual counter value into the latch register. This input is activated by the control bit EN_LATEXT ("1"). EN_LACT has to be deactivated ("0"). After activation, the first edge transition from 0V to 24V at the latch input takes the actual counter value into the latch register. The control bit EN_LATEXT must be deleted and reset, so that the counter value can be stored again.

The gate input stops the counter. Only 0V or an open connection initializes the counter. 24V stops the counting process.

The latch and gate inputs are 24V.

Overview of Inputs and Outputs:

In-/Output	Type	Function
Signal A and Signal /A	Input, RS 422	Incremental pulse signals for channel A
Signal B and Signal /B	Input, RS 422	Incremental pulse signals for channel B
Signal C and Signal /C	Input, RS 422	Track signal for the index channel of the sensor
Shield	Input	Shield connection for encoder wiring
Sensor 0 V (U_0)	Output, power supply	Ground for sensor signals and supply
Sensor +5 V (U_e)	Output, power supply	5 V supply for encoder
+24 V	Input, power supply	24 V supply voltage for the sensor and data processing
0 V	Input, power supply	Ground for the 24 V supply voltage, internally connected to sensor U_0
Gate	Input, 24 V	24 V input for gate signal
Latch	Input, 24 V	24 V input for Latch signal
Ext. Error	Input, low-side switching	Input for alarm output of sensor

2.1.3.7 Process Image

Using the I/O module 750-631/000-004, a 6 byte input and output process image can be transferred to the fieldbus coupler / controller via one logical channel. The data sent and received is stored in 2 output bytes (D0, D1) and 5 input bytes (D0 ... D4). The output bytes D2 ... D4 are reserved and without function. One control byte (C0) and one status byte (S0) are used to control the data flow.



Attention

The representation of the process data of some I/O modules or their variations in the process image depends on the fieldbus coupler/-controller used. Please take this information as well as the particular design of the respective control/status bytes from the section "Fieldbus Specific Design of the Process Data" included in the description concerning the process image of the corresponding coupler/controller.

Input data		Output data	
S0	Status byte	C0	Control byte
D0	Counter value byte 0 (LSB)	D0	Setpoint value byte 0 (LSB)
D1	Counter value byte 1 (MSB)	D1	Setpoint value byte 1 (MSB)
D2	DIG_INPUT	D2	reserved
D3	Latched value byte 0 (LSB)	D3	reserved
D4	Latched value byte 1 (MSB)	D4	reserved

Data byte D2 (DIG_INPUT)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	Signal Input A, /A	Signal Input B, /B	Signal Input C, /C	Signal Input Ext. Error	Signal Input Latch	Signal Input Gate

Signal (0): $U \leq 5.0 \text{ V}$
 Input Gate (1): $U \geq 15.0 \text{ V}$
 Signal (0): $U \leq 5.0 \text{ V}$
 Input Latch (1): $U \geq 15.0 \text{ V}$
 Signal (0): $U \geq 5.0 \text{ V}$ or open connection
 Input (1): $U < 0.5 \text{ V}$
 Ext. Error
 Signal (0): $U_C = 0 \text{ V}$, $U_{/C} = 5 \text{ V}$
 Input C, /C (1): $U_C = 5 \text{ V}$, $U_{/C} = 0 \text{ V}$
 Signal (0): $U_B = 0 \text{ V}$, $U_{/B} = 5 \text{ V}$
 Input B, /B (1): $U_B = 5 \text{ V}$, $U_{/B} = 0 \text{ V}$
 Signal (0): $U_A = 0 \text{ V}$, $U_{/A} = 5 \text{ V}$
 Input A, /A (1): $U_A = 5 \text{ V}$, $U_{/A} = 0 \text{ V}$
 X reserved

Control byte C0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	CNT_SET	EN_LATEXT	EN_LATC

EN_LATC The counter is set with a rising edge of CNT_SET to the value that is specified via the process data.
 EN_LATEXT The external latch input is activated. With the first external latch pulse after validity of the EN_LATEXT bit, the counter value is stored in the latch register. The following pulses have no influence on the latch register when the bit is set.
 CNT_SET The zero point latch (C input) is activated. With the first external latch pulse after the validity of the EN_LATC bit, the counter value is stored in the latch register (this has priority over EN_LATEXT). The following pulses have no influence on the latch register when the bit is set.
 0 reserved

Status byte S0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	OVER- FLOW	UNDER- FLOW	CNTSET _ACK	LA- TEXT_ VAL	LATC_ VAL

LATC_VAL A zero point latch has occurred. The data D3, D4 in the process image corresponds to the latched counter value when the bit is set. To reactivate the latch input, EN_LATC must first be cancelled and then the bit must be set again.

LATEXT_VAL An external latch pulse has occurred. The data D3, D4 in the process image corresponds to the latched counter value when the bit is set. To reactivate the latch input, EN_LATEXT must first be cancelled and then the bit must be set again.

CNTSET_ACK The data for setting the counter has been accepted from the module.

UNDER-FLOW This bit is set if an underflow (0 to 65535) of the 16-bit counter occurs. It is reset when the counter drops below two thirds of the measurement range (43690 to 43689) or as soon as an overflow occurs.

OVER-FLOW This bit is set if an overflow (65535 to 0) of the 16-bit counter occurs. It is reset if the counter exceeds a third of the measurement range (21845 to 21846) or as soon as an underflow occurs.
0 reserved

The following tasks can be performed or checked via the control and status byte:

Extending the counter above 16 bits:

The internal counter has a width of 16 bits. Should the application require an extended range for the location values, the extended counter range may be calculated within the control system using the location-difference-integration method. This method uses the control system to store the last location value (counter value). Any new location value will have the previously stored counter value subtracted from it. Using the sign bit, this difference will be completed with the desired number of extension bits and then be added to the accumulated location value. It is assumed that the counter difference of the two counter queries is smaller than (16-1) bits therefore counter overflows need not be considered.

Another method calculates the counter extension separately by adding the bit OVERFLOW (status bit 4) or subtracting the bit UNDERFLOW (status bit 3) once, each time the counter value is read. Between two counter queries, the counter value should not be increased or decreased by more than $1/3 \times 0xFFFF$. Due to the separate calculation of the counter extension, this procedure allows for calculation using smaller data widths.

Setting the counter value:

Presetting the counter value is possible via the CNT_SET bit (control bit 2). The new counter value is transferred in the load value. When the CNT_SET bit is set from "0" to "1", the counter is loaded with the load value. The CNTSET_ACC bit (status bit 2) is set to "1" when the loading is completed

Maintaining the present counter value:

The present counter value may be maintained or latched via the external latch input. To do so, the EN_LATEXT bit (control bit 1) is set in the control word. Upon transition from "0" to "1", the latch value will contain the counter value at the time of the edge transition. Upon completion of the latch process the LATEXT_VAL bit (status bit 1) will be set to "1". Calculating the extended latch value is done as shown above.

Maintaining a reference point:

The storage of a present counter value may also be accomplished via the index pulse from the encoder. Releasing is done when the EN_LATC bit (control bit 0) is set to "1". The storage of the counter value is completed when LATC_VAL = 1 (status bit 0).

2.1.4 750-631/000-010, 750-631/000-011 [Incremental Encoder Interface]

Incremental Encoder Interface

2.1.4.1 Variations

Item-No.	Designation	Description
750-631/000-010	Increment.Enc.	Incremental Encoder Interface, 4-fold report
750-631/000-011	Increment.Enc./single report	Incremental Encoder Interface, single report

2.1.4.2 View

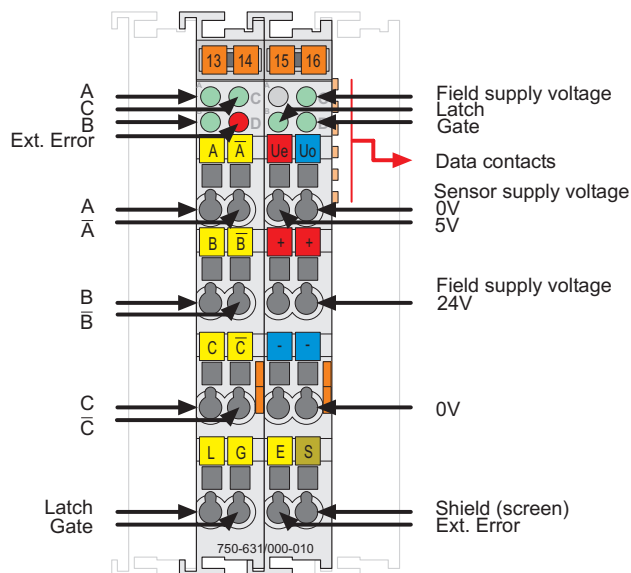


Fig. 2.1.4-1: View

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2.1.4.3 Description

This module is an interface for the connection of following incremental encoder:

- A) Incremental encoder with RS422 output,
- B) Incremental encoder with 24 V push-pull output,
- C) Incremental encoder with non-equivalent 24 V push-pull output,
- D) Incremental encoder with 5 V push-pull output.

The directly connected to the Ue and U0 terminations of the module, the power supply for 24 V transmitter can be connected to the 24 V field supply connectors.

The shield (screen) is directly connected to the carrier rail.

A 16 bit counter with quadrature encoder interface as well as a 16 bit latch for the zero impulse can be read, set, or enabled. The count of the counter will be transmitted fast and interference-free over the fieldbus to the PC, PLC, or NC.

A counter lock-out is possible using input Gate.

Individual green status LEDs indicate the operating status of the module and the signal status of the A, B and C as well as latch and gate inputs and power supply.

A red LED indicates the status of the input for an external error.

Any configuration of the specialty modules is possible when designing the fieldbus node. Grouping of module types is not necessary.



Attention

This module has no power contacts. For field supply to downstream I/O modules, a supply module will be needed.

The module 750-631 and its variations can be used with all couplers/controllers of the WAGO-I/O-SYSTEM 750 (except for the economy types 750-320, -323, -324 and -327).

This description is valid for the XXXX3E08... hardware and software versions. The version is specified in the manufacturing number, which is part of the lateral marking on the module.

2.1.4.4 Display Elements

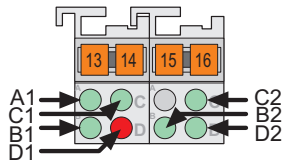


Fig. 2.1.4-2: Display Elements
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LED	Channel	State	Function
A1 green	A	off	Signal voltage (0), (see technical data)
		on	Signal voltage (1), (see technical data)
B1 green	B	off	Signal voltage (0), (see technical data)
		on	Signal voltage (1), (see technical data)
C1 green	C	off	Signal voltage (0), (see technical data)
		on	Signal voltage (1), (see technical data)
D1 red	Ext. Error	off	$U \geq 5.0 \text{ V}$ or open connection
		on	$U < 0.5 \text{ V}$
B2 green	Latch	off	$U \leq 5.0 \text{ V}$
		on	$U \geq 15.0 \text{ V}$
C2 green	Field supply	off	24 V field supply voltage missing
		on	24 V field supply voltage ok
D2 green	Gate	off	$U \leq 5.0 \text{ V}$
		on	$U \geq 15.0 \text{ V}$

2.1.4.5 Schematic Diagram

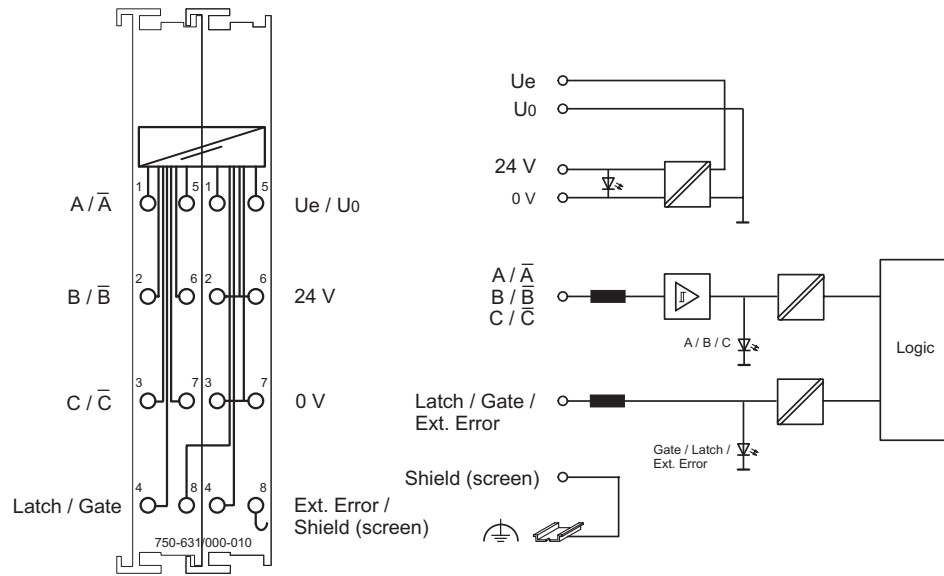






Fig. 2.1.4-2: Schematic Diagram

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2.1.4.6 Technical Data

Module Specific Data		
Sensor connection	Variation A	Incremental encoder with RS422 output
	Variation B	Incremental encoder with 24 V push-pull output
	Variation C	Incremental encoder with non-equivalent 24 V push-pull output
	Variation D	Incremental encoder with 5 V push-pull output
Signal voltage A, B, C, /A, /B, /C	Variation A	(0): $U_{A,B,C} = 0 \text{ V}$, $U_{/A,/B,/C} = 5 \text{ V}$ (1): $U_{A,B,C} = 5 \text{ V}$, $U_{/A,/B,/C} = 0 \text{ V}$
	Variation B	(0): $U_{A,B,C} \leq 5 \text{ V}$ (1): $U_{A,B,C} \geq 15 \text{ V}$
	Variation C	(0): $U_{A,B,C} = 0 \text{ V}$, $U_{/A,/B,/C} = 5 \text{ V}$ (1): $U_{A,B,C} = 5 \text{ V}$, $U_{/A,/B,/C} = 0 \text{ V}$
	Variation D	(0): $U_{A,B,C} \leq 5 \text{ V}$ (1): $U_{A,B,C} \geq 15 \text{ V}$
Signal voltage Latch, Gate		(0) $U \leq 5.0 \text{ V}$ (1) $U \geq 15.0 \text{ V}$
Signal voltage Ext. Error		(0) $U \geq 5.0 \text{ V}$ or open connection (1) $U < 0.5 \text{ V}$
Sensor power supply		DC 5 V
Sensor output current i_{max}		200 mA
Counter		16 bits binary
Operating frequency		1 MHz
Quadrature decoder		4-fold report (750-631/000-010), single report (750-631/000-011)
Zero impulse latch		16 bits
Commands		read, set, enable
Voltage supply		DC 24 V (-15 % ... +20 %)
Current consumption (internal)		50 mA
Current consumption (field) $_{\text{typ}}$		10 mA without sensor
Internal bit width		1 x 32 bits 1 x 8 bits control/status 1 x 8 bits reserved
Isolation		500 V (System/Supply)
Dimensions W x H* x L * from upper edge of 35 DIN rail		24 mm x 64 mm x 100 mm
Weight		ca. 105 g

Approvals (cf. Chapter 2.2 of the Coupler/Controller Manual)		
	cUL _{US} (UL508)	
	cUL _{US} (UL1604)	Class I Div2 ABCD T4A
	KEMA	II 3 G EEx nA II T4
	Conformity Marking	



More Information

Detailed references to the approvals are listed in the document "Overview Approvals WAGO-I/O-SYSTEM 750", which you can find on the CD ROM ELECTRONICC Tools and Docs (Item-No.: 0888-0412)

or in the internet under:

www.wago.com → Documentation → WAGO-I/O-SYSTEM 750 → System Description

2.1.4.7 Functional Description

The incremental encoder interface is used to evaluate two 90° phase-shifted track signals delivered by digital encoders with 5 V ... 24 V output. If required, the signals generated by the index track can also be processed. Control via two 24V signals is optional.

Typically, incremental encoders provide two signals of the encoder track, both 90° offset. These signals are labelled A and B.

In the case of connector versions A and C, the signals are transmitted as differential signals for an improved common mode rejection. Besides signal A, the inverted level /A is also transmitted. The difference of the input signals is formed in the incremental encoder interface.

By exchanging A and /A the phase position will turn from A to B, thus allowing the desired counting direction to be preset via the wiring configuration.

Connector versions B and D are also known as S.E. (single ended). The potentials of the track signals relate to the common earth connection. In comparison to the complementary evaluation of the track signals, the susceptibility is higher because common-mode interferences are not suppressed.

Most incremental encoders have an index track in addition to the two track signals. This index track generates a single pulse per encoder revolution. This pulse can be used to determine the absolute encoder position within a revolution. Through the appropriate initialization, the current counter value is transmitted to a latch register using the index pulse. Since the index pulse has the same duration as a track signal, the latch process should always be performed in the same rotational direction.

If the rotary transducer is equipped with a monitoring electronics with NPN alarm output, then this output can be connected to the external error [input](#). The input is switching negatively, i.e., 0V is logically mapped to 1.

With connector versions A and D, the 5V supply for the sensor can be tapped off at the outputs Ue and U0. This supply voltage is generated from 24V to be provided externally. The inputs 0V and U0 are connected internally.

The latch input controls the overtaking of the actual counter value into the latch register. This input is activated by the control bit EN_LATEXT ("1"). EN_LACT has to be deactivated ("0"). After activation, the first edge transition from 0V to 24V at the latch input takes the actual counter value into the latch register. The control bit EN_LATEXT must be deleted and reset, so that the counter value can be stored again.

The gate input stops the counter. Only 0V or an open connection initialize the counter. 24V stops the counting process.

The latch and gate inputs are 24V.

Overview of Inputs and Outputs:

In-/Output	Type	Function
Signal A and Signal /A	Input	Incremental pulse signals for channel A
Signal B and Signal /B	Input	Incremental pulse signals for channel B
Signal C and Signal /C	Input	Track signal for the index channel of the sensor
Shield	Input	Shield connection for encoder wiring
Sensor 0 V (U_0)	Output, power supply	Ground for sensor signals and supply
Sensor +5 V (U_e)	Output, power supply	5 V supply for encoder
+24 V	Input, power supply	24 V supply voltage for the sensor and data processing
0 V	Input, power supply	Ground for the 24 V supply voltage, internally connected to sensor U_0
Gate	Input, 24 V	24 V input for gate signal
Latch	Input, 24 V	24 V input for Latch signal
Ext. Error	Input, low-side switching	Input for alarm output of sensor

2.1.4.8 Process Image

Using the I/O module 750-631/000-010 or 750-631/000-011, a 6 byte input and output process image can be transferred to the fieldbus coupler / controller via one logical channel. The data sent and received is stored in 2 output bytes (D0, D1) and 5 input bytes (D0 ... D4). The output bytes D2 ... D4 are reserved and without function. One control byte (C0) and one status byte (S0) are used to control the data flow.



Attention

The representation of the process data of some I/O modules or their variations in the process image depends on the fieldbus coupler/-controller used. Please take this information as well as the particular design of the respective control/status bytes from the section "Fieldbus Specific Design of the Process Data" included in the description concerning the process image of the corresponding coupler/controller.

Input data		Output data	
S0	Status byte	C0	Control byte
D0	Counter value byte 0 (LSB)	D0	Setpoint value byte 0 (LSB)
D1	Counter value byte 1 (MSB)	D1	Setpoint value byte 1 (MSB)
D2	DIG_INPUT	D2	reserved
D3	Latched value byte 0 (LSB)	D3	reserved
D4	Latched value byte 1 (MSB)	D4	reserved

Data byte D2 (DIG_INPUT)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	Signal Input A, /A	Signal Input B, /B	Signal Input C, /C	Signal Input Ext. Error	Signal Input Latch	Signal Input Gate

Signal (0): $U \leq 5.0 \text{ V}$
 Input Gate (1): $U \geq 15.0 \text{ V}$
 Signal (0): $U \leq 5.0 \text{ V}$
 Input Latch (1): $U \geq 15.0 \text{ V}$
 Signal (0): $U \geq 5.0 \text{ V}$ or open connection
 Input (1): $U < 0.5 \text{ V}$
 Ext. Error
 Signal (0): Signal voltage (0), (see technical data)
 Input C, /C (1): Signal voltage (1), (see technical data)
 Signal (0): Signal voltage (0), (see technical data)
 Input B, /B (1): Signal voltage (1), (see technical data)
 Signal (0): Signal voltage (0), (see technical data)
 Input A, /A (1): Signal voltage (1), (see technical data)
 X reserved

Control byte C0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	CNT_SET	EN_LATEXT	EN_LATC

EN_LATC The counter is set with a rising edge of CNT_SET to the value that is specified via the process data.
 EN_LATEXT The external latch input is activated. With the first external latch pulse after validity of the EN_LATEXT bit, the counter value is stored in the latch register. The following pulses have no influence on the latch register when the bit is set.
 CNT_SET The zero point latch (C input) is activated. With the first external latch pulse after the validity of the EN_LATC bit, the counter value is stored in the latch register (this has priority over EN_LATEXT). The following pulses have no influence on the latch register when the bit is set.
 0 reserved

Status byte S0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	OVER- FLOW	UNDER- FLOW	CNTSET _ACK	LA- TEXT_ VAL	LATC_ VAL

LATC_VAL A zero point latch has occurred. The data D3, D4 in the process image corresponds to the latched counter value when the bit is set. To reactivate the latch input, EN_LATC must first be cancelled and then the bit must be set again.

LATEXT_VAL An external latch pulse has occurred. The data D3, D4 in the process image corresponds to the latched counter value when the bit is set. To reactivate the latch input, EN_LATEXT must first be cancelled and then the bit must be set again.

CNTSET_ACK The data for setting the counter has been accepted from the module.

UNDER-FLOW This bit is set if an underflow (0 to 65535) of the 16-bit counter occurs. It is reset when the counter drops below two thirds of the measurement range (43690 to 43689) or as soon as an overflow occurs.

OVER-FLOW This bit is set if an overflow (65535 to 0) of the 16-bit counter occurs. It is reset if the counter exceeds a third of the measurement range (21845 to 21846) or as soon as an underflow occurs.

0 reserved

The following tasks can be performed or checked via the control and status byte:

Extending the counter above 16 bits:

The internal counter has a width of 16 bits. Should the application require an extended range for the location values, the extended counter range may be calculated within the control system using the location-difference-integration method. This method uses the control system to store the last location value (counter value). Any new location value will have the previously stored counter value subtracted from it. Using the sign bit, this difference will be completed with the desired number of extension bits and then be added to the accumulated location value. It is assumed that the counter difference of the two counter queries is smaller than (16-1) bits therefore counter overflows need not be considered.

Another method calculates the counter extension separately by adding the bit OVERFLOW (status bit 4) or subtracting the bit UNDERFLOW (status bit 3) once, each time the counter value is read. Between two counter queries, the counter value should not be increased or decreased by more than $1/3 \times 0xFFFF$. Due to the separate calculation of the counter extension, this procedure allows for calculation using smaller data widths.

Setting the counter value:

Presetting the counter value is possible via the CNT_SET bit (control bit 2). The new counter value is transferred in the load value. When the CNT_SET bit is set from "0" to "1", the counter is loaded with the load value. The CNTSET_ACC bit (status bit 2) is set to "1" when the loading is completed.

Maintaining the present counter value:

The present counter value may be maintained or latched via the external latch input. To do so, the EN_LATEXT bit (control bit 1) is set in the control word. Upon transition from "0" to "1", the latch value will contain the counter value at the time of the edge transition. Upon completion of the latch process the LATEXT_VAL bit (status bit 1) will be set to "1". Calculating the extended latch value is done as shown above.

Maintaining a reference point:

The storage of a present counter value may also be accomplished via the index pulse from the encoder. Releasing is done when the EN_LATC bit (control bit 0) is set to "1". The storage of the counter value is completed when LATC_VAL = 1 (status bit 0).

2.1.4.9 Connection Variations

2.1.4.9.1 Incremental Encoder with RS422 Output (Variation A)

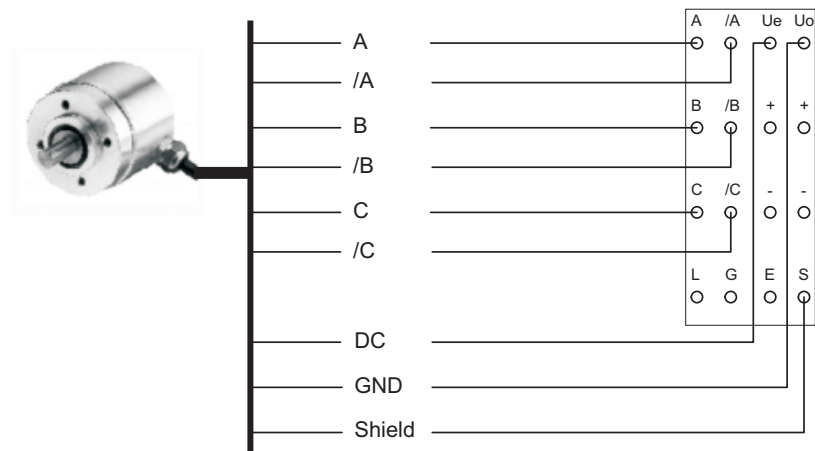


Abb. 2.1.4-3: Incremental encoder with RS422 output

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2.1.4.9.2 Incremental Encoder with 24 V Push-Pull Output (Variation B)

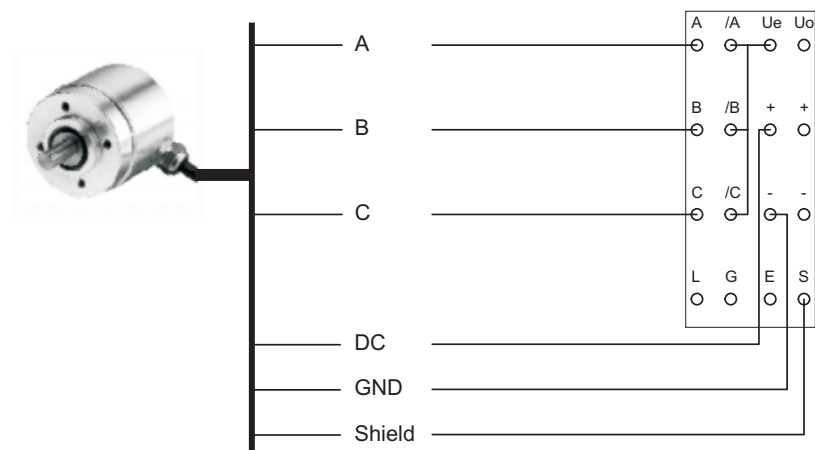


Abb. 2.1.4-4: Incremental encoder with 24 V push-pull output

g0631a4e

2.1.4.9.3 Incremental Encoder with non-equivalent 24 V Push-Pull Output (Variation C)

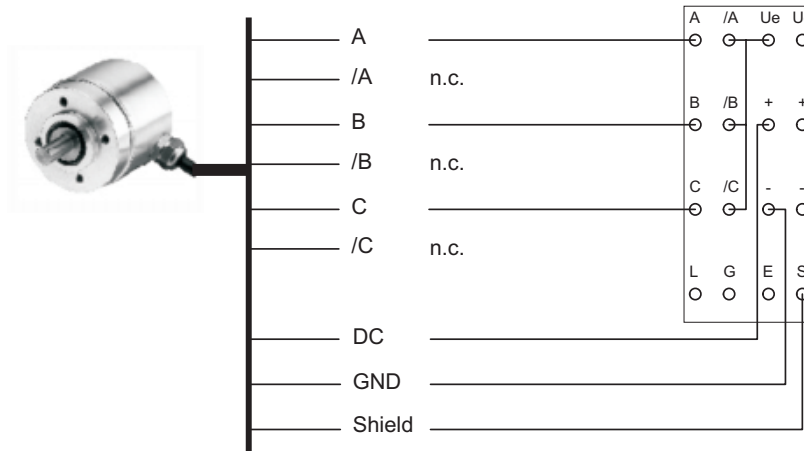


Abb. 2.1.4-5: Incremental encoder with non-equivalent 24 V push-pull output

g0631a5e

2.1.4.9.4 Incremental Encoder with 5 V Push-Pull Output (Variation D)

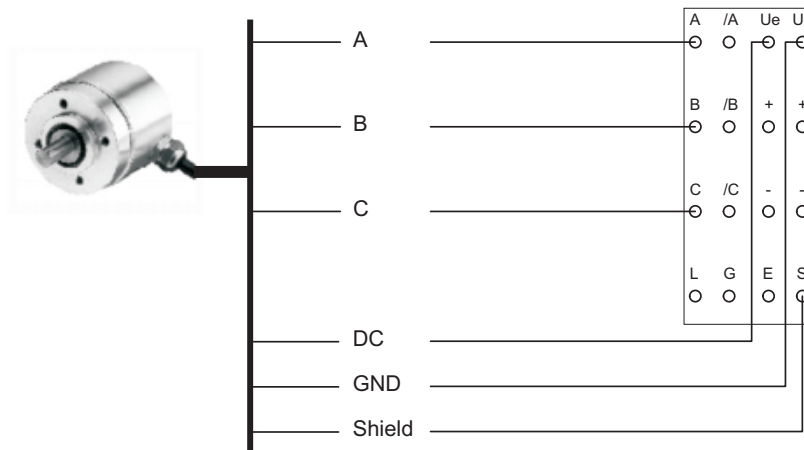


Abb. 2.1.4-6: Incremental encoder with 5 V push-pull output

g0631a6e



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