

**WAGO → I/O → SYSTEM 750**

**Fieldbus Independent  
I/O Modules**

**Incremental Encoder Interfaces  
750-637, (/xxx-xxx)**



**Manual**

Version 1.3.2

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Every conceivable measure has been taken to ensure the correctness and completeness of this documentation. However, as errors can never be fully excluded, we would appreciate any information or ideas at any time.

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We wish to point out that the software and hardware terms as well as the trademarks of companies used and/or mentioned in the present manual are generally trademark or patent protected.

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# 1 Important Comments

To ensure fast installation and start-up of the units described in this manual, we strongly recommend that the following information and explanations are carefully read and abided by.

## 1.1 Legal Principles

### 1.1.1 Copyright

This manual is copyrighted, together with all figures and illustrations contained therein. Any use of this manual which infringes the copyright provisions stipulated herein, is not permitted. Reproduction, translation and electronic and photo-technical archiving and amendments require the written consent of WAGO Kontakttechnik GmbH & Co. KG. Non-observance will entail the right of claims for damages.

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### 1.1.2 Personnel Qualification

The use of the product detailed in this manual is exclusively geared to specialists having qualifications in PLC programming, electrical specialists or persons instructed by electrical specialists who are also familiar with the valid standards. WAGO Kontakttechnik GmbH & Co. KG declines all liability resulting from improper action and damage to WAGO products and third party products due to non-observance of the information contained in this manual.

### 1.1.3 Intended Use

For each individual application, the components supplied are to work with a dedicated hardware and software configuration. Modifications are only permitted within the framework of the possibilities documented in the manuals. All other changes to the hardware and/or software and the non-conforming use of the components entail the exclusion of liability on part of WAGO Kontakttechnik GmbH & Co. KG.

Please direct any requirements pertaining to a modified and/or new hardware or software configuration directly to WAGO Kontakttechnik GmbH & Co. KG.

## 1.2 Symbols



### **Danger**

Always abide by this information to protect persons from injury.



### **Warning**

Always abide by this information to prevent damage to the device.



### **Attention**

Marginal conditions must always be observed to ensure smooth operation.



### **ESD (Electrostatic Discharge)**

Warning of damage to the components by electrostatic discharge. Observe the precautionary measure for handling components at risk.



### **Note**

Routines or advice for efficient use of the device and software optimization.



### **More information**

References on additional literature, manuals, data sheets and INTERNET pages

## 1.3 Number Notation

Number Code	Example	Note
Decimal	100	normal notation
Hexadecimal	0x64	C notation
Binary	'100' '0110.0100'	Within ', Nibble separated with dots

## 1.4 Safety Notes



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### Warning

Switch off the system prior to working on bus modules!

In the event of deformed contacts, the module in question is to be replaced, as its functionality can no longer be ensured on a long-term basis.

The components are not resistant against materials having seeping and insulating properties. Belonging to this group of materials is: e.g. aerosols, silicones, triglycerides (found in some hand creams).

If it cannot be ruled out that these materials appear in the component environment, then additional measures are to be taken:

- installation of the components into an appropriate enclosure
  - handling of the components only with clean tools and materials.
- 



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### Attention

Cleaning of soiled contacts may only be done with ethyl alcohol and leather cloths. Thereby, the ESD information is to be regarded.

Do not use any contact spray. The spray may impair the functioning of the contact area.

The WAGO-I/O-SYSTEM 750 and its components are an open system. It must only be assembled in housings, cabinets or in electrical operation rooms. Access must only be given via a key or tool to authorized qualified personnel.

The relevant valid and applicable standards and guidelines concerning the installation of switch boxes are to be observed.

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### ESD (Electrostatic Discharge)

The modules are equipped with electronic components that may be destroyed by electrostatic discharge. When handling the modules, ensure that the environment (persons, workplace and packing) is well grounded. Avoid touching conductive components, e.g. gold contacts.

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## 1.5 Scope

This manual describes the special modules 750-637, (/xxx-xxx)  
Incremental Encoder Interfaces of the modular WAGO-I/O-SYSTEM 750.

Handling, assembly and start-up are described in the manual of the Fieldbus Coupler. Therefore this documentation is valid only in the connection with the appropriate manual

## 2 I/O Modules

### 2.1 Special Modules

#### 2.1.1 Overview Incremental Encoder Interfaces 750-637, (/xxx-xxx)

I/O Module	<a href="#">750-637</a>	<a href="#">750-637/ 000-001</a>	<a href="#">750-637/ 000-002</a>	<a href="#">750-637/ 000-003</a>
Function	Incremental Encoder Interface	Incremental Encoder Interface	Incremental Encoder Interface	Incremental Encoder Interface
Input	differential	differential	single ended	differential
Sensor Operation Voltage	DC 5 V	DC 24 V	DC 24 V	DC 5 V
Interpretation	fourfold	fourfold	fourfold	single
Bit Width	32 Bit	32 Bit	32 Bit	32 Bit

## 2.1.2 750-637 [Inc.Enc./RS422/32Bit/Diff.]

Incremental encoder interface RS422 / 32 bit / differential

### 2.1.2.1 View

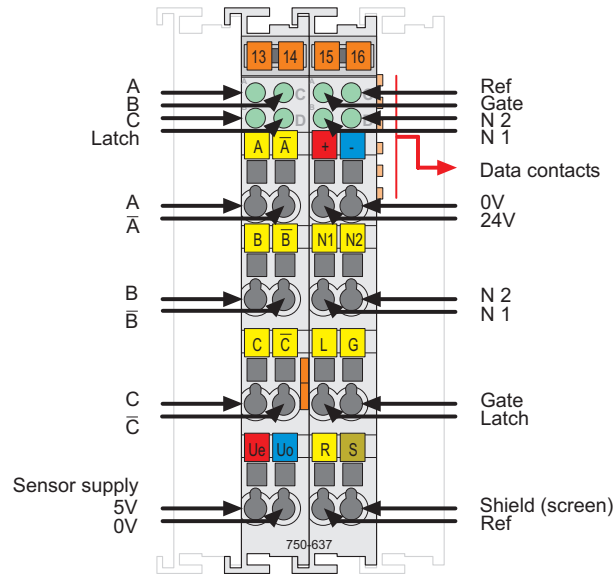


Fig. 2.1.2-1: View

g063700e

### 2.1.2.2 Variations

Item-No.	Designation	Description
750-637	Inc.Enc./RS422/32Bit/Diff.	Incremental Encoder Interface RS422 / 32 Bit / differential / fourfold interpretation
750-637/000-003	Inc.Enc./RS422/32Bit/Diff./Single Interpret.	Incremental Encoder Interface RS422 / 32 Bit / differential / single interpretation

### 2.1.2.3 Description

The I/O module 750-637 represents an interface for any type of incremental encoder with an RS 422 connection.

The data width of the encoder module is 32 bits. Either the current counter reading, the latch value, the set value or the current speed can be mapped into the process data.

Inputs/Outputs	
A, /A, B, /B	Quadrature input, RS 422
C, /C	Zero reference input, RS 422
Latch, Gate, Ref	Input, 24 V
N1, N2	Output, 24 V

A counter with quadrature decoder and a latch for the zero pulse can be read and activated by the PLC. The PLC is able to set the counter. Depending on the operating mode, the counter reading is taken into the latch register, if the edge at input “C” or “Latch” is positive.

The speed (increments/ms) is automatically recorded and can be transmitted as an alternative to the latch value.

The „Gate” input allows to lock the counter. The „Ref” input can be set to activate the zero mark „C”.

The cam outputs N1 and N2 indicate whether the counter value is within a defined range of values. The range can be adjusted for each cam via the PLC. Starting with the software version XXXX03XX, the cam outputs can be disabled by the PLC and the states of the cam outputs can be queried.

24 V DC is required to supply the I/O modules, from this voltage also the voltage supply to the encoder (Ue, U0) is branched/tapped.



#### Attention

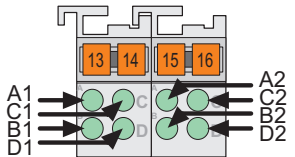
This module has no power contacts. For field supply to downstream I/O modules, a supply module will be needed.

The shield (screen) is directly connected to the carrier rail.

The module 750-637 can be used with all couplers/controllers of the WAGO-I/O-SYSTEM 750 (except for the economy types 750-320, -323, -324 and -327).

The version of both hardware and software that are valid for this module is specified in the manufacturing number, which is part of the lateral marking on the module.

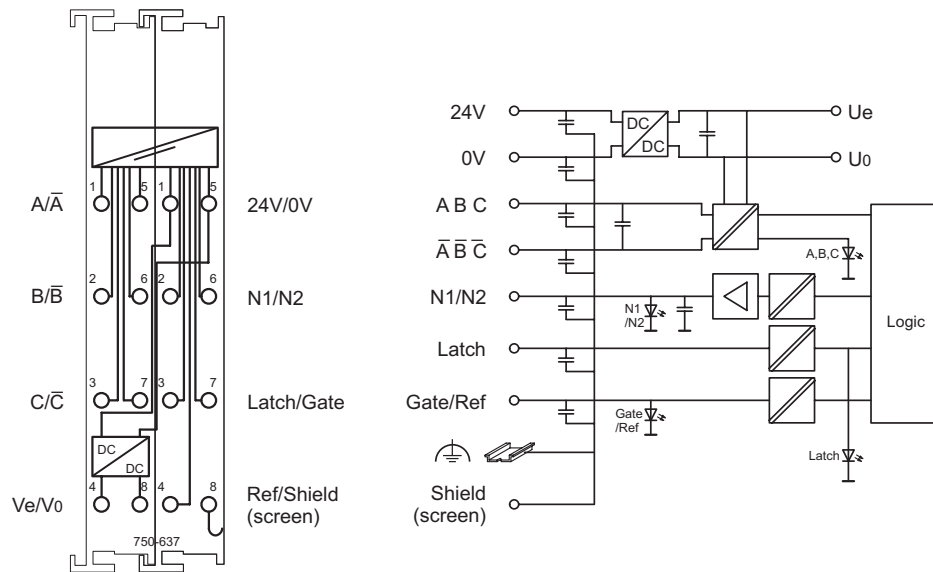
### 2.1.2.4 Display Elements



LED	Designation	Status	Function
A1 green	A	off	$U(A) - U(/A) < -0,2 \text{ V}$
		on	$U(A) - U(/A) > 0,2 \text{ V}$ or both inputs open
B1 green	C	off	$U(C) - U(/C) < -0,2 \text{ V}$
		on	$U(C) - U(/C) > 0,2 \text{ V}$ or both inputs open
C1 green	B	off	$U(B) - U(/B) < -0,2 \text{ V}$
		on	$U(B) - U(/B) > 0,2 \text{ V}$ or both inputs open
D1 green	Latch	off	Input = 0 V or open
		on	Input = 24 V
A2 green	Gate	off	Input = 0 V or open
		on	Input = 24 V
B2 green	N1	off	Output = 0 V
		on	Output = 24 V
C2 green	Ref	off	Input = 0 V or open
		on	Input = 24 V
D2 green	N2	off	Output = 0 V
		on	Output = 24 V





Fig. 2.1.2-2: Display elements g063702x

### 2.1.2.5 Schematic Diagram



## 2.1.2.6 Technical Data

<b>Module specific Data</b>	
Sensor connection	A, /A, B, /B, C, /C (/A, /B, /C are inversed)
Current consumption (internal)	110 mA
Counter	32 bits binary
Operation Mode Capture	32 bits
Operation Mode Preload	32 bits
Quadrature decoder	fourfold interpretation (750-637) single interpretation (750-637/000-003)
Zero impulse latch	32 bits
Commands	read, write, activate
Velocity	16 Bit (increments per 1ms)
Max. operating frequency	250 kHz
Time constant input LATCH	364 $\mu$ s
Time constant input GATE	32 $\mu$ s
Time constant input REF	32 $\mu$ s
Power supply	DC 24 V (- 15 % ... + 20 %)
Current consumption (24 V)	12 mA (without sensor and without load)
Sensor Operation voltage	DC 5 V
Sensor Output current <sub>max</sub>	300 mA
Internal bit width	1 x 32 bits data 2 x 8 bits control / status
Dimensions W x H* x L * from upper edge of DIN 35 rail	24 mm x 64 mm x 100 mm
Weight	ca. 105 g
<b>Digital Outputs (N1, N2)</b>	
Output voltage	DC 24 V
Output current <sub>max.</sub>	0,5 A short-circuit-protected
Output resistance <sub>typ.</sub>	160 m $\Omega$
<b>Digital Inputs (Latch, Gate, Ref)</b>	
Input voltage	(0) DC -3 V ... +5 V (1) DC +15 V ... +30 V
Input current <sub>typ.</sub>	Latch: 5 mA Gate and Ref: 7 mA

<b>Quadrature Inputs (A, /A, B, /B, C, /C)</b>		
Input voltage A, /A	(0) $U(A) - U(/A) < -0,2 \text{ V}$ (1) $U(A) - U(/A) > 0,2 \text{ V}$	
Input voltage B, /B	(0) $U(B) - U(/B) < -0,2 \text{ V}$ (1) $U(B) - U(/B) > 0,2 \text{ V}$	
Input voltage C, /C	(0) $U(C) - U(/C) < -0,2 \text{ V}$ (1) $U(C) - U(/C) > 0,2 \text{ V}$	
<b>Standards and Regulations (cf. Chapter 2.2 of the Coupler/Controller Manual)</b>		
EMC-Immunity to interference (CE)	acc. to EN 50082-2 (96)	
EMC-Emission of interference (CE)	acc. to EN 50081-1 (93)	
<b>Approvals (cf. Chapter 2.2 of the Coupler/Controller Manual)</b>		
	cUL <sub>US</sub> (UL508)	
	cUL <sub>US</sub> (UL1604)	Class I Div2 ABCD T4A
	DEMKO	II 3 GD EEx nA II T4
	Conformity Marking	



**More Information**

Detailed references to the approvals are listed in the document "Overview Approvals WAGO-I/O-SYSTEM 750", which You can find on the CD ROM ELECTRONICC Tools and Docs (Item-No.: 0888-0412/...) or in the Internet under:

[www.wago.com](http://www.wago.com) -> Service /Downloads /Documentation /WAGO-I/O-SYSTEM 750/System Description/.

Further „General Technical Data“ for the WAGO-I/O-SYSTEM 750 is available in the specific fieldbus coupler / controller manuals.

### 2.1.2.7 Functional Description

Typically, incremental encoders supply two output signals of the encoder track, both 90° offset. These signals are designated A and B. To improve the common mode interference suppression, both signals are transmitted as differential signals. In addition to the A signal, also the inverted /A level is transmitted. The difference of the input signals is evaluated in the incremental encoder I/O module. The phase position changes from A to B by changing A and /A. In this manner, it is possible to pre-define the desired counting direction by wiring.

Usually, incremental encoders have an index track in addition to the two track signals. This index track only produces one pulse per one full encoder revolution. This pulse and the counter reading can be used to determine the absolute encoder position during rotation. The index pulse has a duration of a track position pulse. We recommend to always have the latch process performed in the same rotational direction.

<b>Input</b>	<b>Function</b>
A, /A, B, /B	Quadrature input, RS 422 Increment pulse signal channel A or B of the Incremental Encoder
C, /C	Zero reference input, RS 422 Incremental encoder index pulse Dependent on the operating mode, the counter reading is taken over into the latch register or the counter showing the set value is additionally loaded, if the input edge is positive.
LATCH	LATCH input 24 V Dependent on the operating mode, the counter reading is taken into the latch register or the counter showing the set value is additionally loaded, if the input edge is positive.
GATE	GATE input, 24 V The counting process is locked if 24 V is applied to input GATE.
REF	REF input, 24 V During a reference run, the index pulse is only evaluated in conjunction with an additional sensor signal (Ref).
Screen (Shield)	Connection for the encoder line screen The screen connection is directly routed to the carrier rail.
Ue (+5V)	5 V supply output for the sensor
U <sub>0</sub> (0V)	Ground for the sensor signal and supply, internally connected with 0 V
+24V	24 V supply voltage for the module
0V	Ground for the 24 V supply voltage, internally connected with U <sub>0</sub> .
<b>Output</b>	<b>Function</b>
N1, N2	Cam output, 24 V, 0.5 A "1" - Counter value is within of the defined range "0" - Counter value is outside of the defined range

### 2.1.2.8 Process Image

Using the I/O module 750-637, a 6 byte input and output process image can be transferred to the fieldbus coupler / controller via two logical channels.

The set values are stored in 4 output bytes (D0, D1, D2, D3) and the process data are stored in 4 input bytes (D0, D1, D2, D3). Two control bytes (C0, C1) and two status bytes (S0, S1) are used to select process data and set values as well as to control the data flow.



#### Attention

The representation of the process data of some I/O modules or their variations in the process image depends on the fieldbus coupler/-controller used. Please take this information as well as the particular design of the respective control/status bytes from the section "Fieldbus Specific Design of the Process Data" included in the description concerning the process image of the corresponding coupler/controller.

Input data		Output data	
S0	Status byte S0	C0	Control byte C0
D0	Process data byte 0 (LSB)	D0	Set value byte 0 (LSB)
D1	Process data byte 1	D1	Set value byte 1
S1	Status byte S1	C1	Control byte C1
D2	Process data byte 2	D2	Set value byte 2
D3	Process data byte 3 (MSB)	D3	Set value byte 3 (MSB)

Bit 0 and bit 1 in the control byte C1 determines the process data.

- Counter value
- Latch value
- Velocity
- Set value

The setting is mirrored in status byte S1 in bit 0 and bit 1.

MapPZD (Control Byte C1 / Status Byte S1, Bit 0 and 1)		
Bit 1	Bit 0	Coding of the Process data
0	0	Counter value
0	1	Latch value
1	0	Velocity (Increments per milliseconds)
1	1	Set value

Status Byte S0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	X	AckSet LoadExt	OVER- FLOW	UNDER- FLOW	CNT_ SET_ ACK	LAT_ EXT_ VAL	LATC_ VAL

LATC_ VAL	Acknowledge bit for EN_LATC (C0.0). Latch Mode: This bit is set with a positive edge at input C. It is reset when EN_LATC is reset. Preload Mode: This bit is set with a positive edge at C. It is reset when EN_LATC is reset.
LAT_ EXT_ VAL	Acknowledge bit for EN_LAT_EXT (C0.1). Latch Mode: This bit is set with a positive edge at the input Latch. It is reset when EN_LAT_EXT is reset. Preload Mode: This bit is set with a positive edge at the input Latch. It is reset when EN_LAT_EXT is reset.
CNT_ SET_ ACK	Acknowledge bit for CNT_SET (C0.2). Reset if CNT_SET=0
UNDER- FLOW	UNDERFLOW=1 with a counter overflow of 0x00000000 to 0xffffffff UNDERFLOW=0 if counter < 0xAAAAAAAA UNDERFLOW=0 if positive edge ResetUnderflow (C1.3) UNDERFLOW=0 if OVERFLOW=1
OVER- FLOW	OVERFLOW=1 with a counter overflow of 0xffffffff to 0x00000000 OVERFLOW=0 if counter > 0x55555555 OVERFLOW=0 if positive edge ResetOverflow (C1.4) OVERFLOW=0 if UNDERFLOW=1
AckSet LoadExt	Acknowledge bit for SetLoadExt. Reset if SetLoadExt=0 (C0.5)
X	reserved
0	reserved

Status Byte S1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	N2	N1	StaN2	StaN1	MapPZD	MapPZD

MapPZD	Software version < XXXX03XX: reserved / not used (0) software version ≥ XXXX03XX: coding of process data (2 Bits)
StaN2	Software version < XXXX03XX: reserved / not used (0) software version ≥ XXXX03XX: state of cam output 1: 0 = cam output 1 reset, 1 = cam output 1 set
StaN1	Software version < XXXX03XX: reserved / not used (0) software version ≥ XXXX03XX: state of cam output 2: 0 = cam output 2 reset, 1 = cam output 2 set
N1	Cam window 1st bit is set, if: bottom comparative value N1 ≤ counter reading ≤ top comparative value N1
N2	Cam window 2nd bit is set, if: bottom comparative value N2 ≤ counter reading ≤ top comparative value N2
0	reserved



Control Byte C1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Enable Ref	Set Nocke2	Set Nocke1	Dis Nocke2	Dis Nocke1	MapPZD	MapPZD

MapPZD Coding of Process data (2 bits)

DisNocke1 Software version < XXXX03XX: reserved / not used (0)  
software version ≥ XXXX03XX: disable cam output 1:  
0 = cam output 1 enabled, 1 = cam output 1 disabled

DisNocke2 Software version < XXXX03XX: reserved / not used (0)  
software version ≥ XXXX03XX: disable cam output 2:  
0 = cam output 2 enabled, 1 = cam output 2 disabled

SetNocke1 With a positive edge, the set value is taken over as the bottom comparative value for output 1 (N1).  
With a negative edge, the set value is taken over as the top comparative value for output 1 (N1).

SetNocke2 With a positive edge, the set value is taken over as bottom comparative value for output 2 (N2).  
With a negative edge, the set value is taken over as top comparative value for output 2 (N2).

EnableRef Input REF released.  
- The controls set Bit EnableRef  
- The controls must release EN\_LATC (C1.0) or EN\_LAT\_EXT (C1.1) with a positive edge  
- A positive edge is created at input REF  
- Subsequently, the next positive edge at input C or input Latch leads to a Capture or Preload event

0 reserved

### 2.1.3 750-637/000-001 [Inc.Enc./24V/32Bit/Diff.]

Incremental encoder interface 24 V / 32 bit / differential

#### 2.1.3.1 View

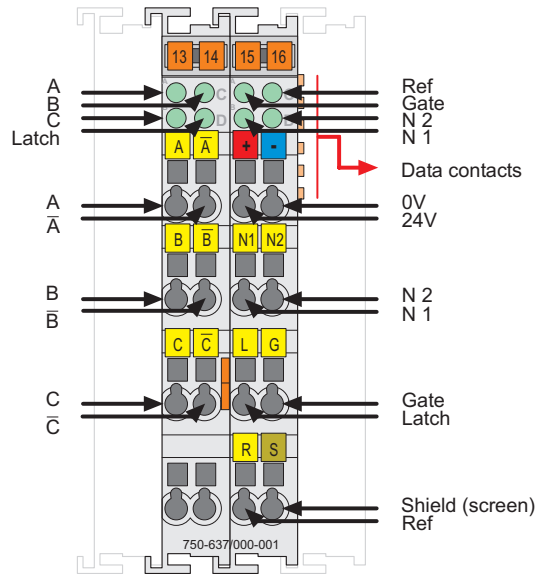


Fig. 2.1.3-1: View

g063710e

#### 2.1.3.2 Description

The I/O module 750-637/000-001 represents an interface for any type of incremental encoder with an differential 24 V connection.

The data width of the encoder module is 32 bits. Either the current counter reading, the latch value, the set value or the current speed can be mapped into the process data.

Inputs/Outputs	
A, /A, B, /B	Quadrature input, 24 V, differential
C, /C	Zero reference input, 24 V, differential
Latch, Gate, Ref	Input, 24 V
N1, N2	Output, 24 V

A counter with quadrature decoder and a latch for the zero pulse can be read and activated by the PLC. The PLC is able to set the counter. Depending on the operating mode, the counter reading is taken into the latch register, if the edge at input “C” or “Latch” is positive.

The speed (increments/ms) is automatically recorded and can be transmitted as an alternative to the latch value.

The „Gate” input allows to lock the counter. The „Ref” input can be set to activate the zero mark „C”.

The I/O module signals whether the counter reading is within the defined set points by using the cam outputs (N1, N2). The set points can be individually set.

The I/O module requires 24 VDC power supply.

The sensor is fed with an external power supply. The sensor ground must be connected to the 0V terminal of the module.



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**Attention**

This module has no power contacts. For field supply to downstream I/O modules, a supply module will be needed.

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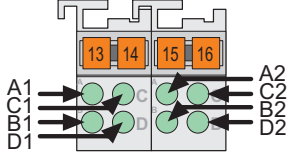
The shield (screen) is directly connected to the carrier rail.

The module 750-637/000-001 can be used with all couplers/controllers of the WAGO-I/O-SYSTEM 750 (except for the economy types 750-320, -323, -324 and -327).

This description is valid for the XXXX0301... hardware and software version. The version is specified in the manufacturing number, which is part of the lateral marking on the module.

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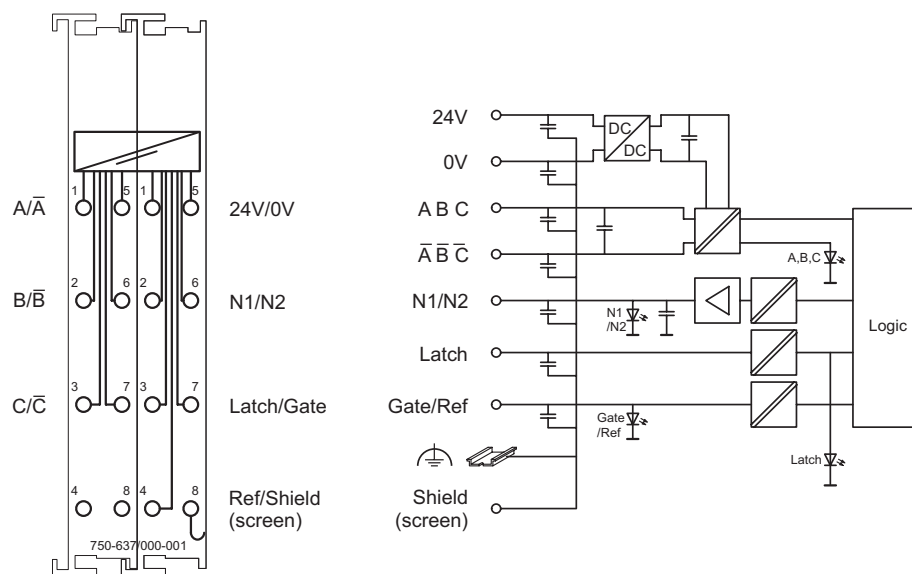
### 2.1.3.3 Display Elements



LED	Designation	Status	Function
A1 green	A	off	$-30\text{ V} < (U(A) - U(/A)) < -15\text{ V}$
		on	$30\text{ V} > (U(A) - U(/A)) > 15\text{ V}$ or both inputs open
B1 green	C	off	$-30\text{ V} < (U(C) - U(/C)) < -15\text{ V}$
		on	$30\text{ V} > (U(C) - U(/C)) > 15\text{ V}$ or both inputs open
C1 green	B	off	$-30\text{ V} < (U(B) - U(/B)) < -15\text{ V}$
		on	$30\text{ V} > (U(B) - U(/B)) > 15\text{ V}$ or both inputs open
D1 green	Latch	off	Input = 0 V or open
		on	Input = 24 V
A2 green	Gate	off	Input = 0 V or open
		on	Input = 24 V
B2 green	N1	off	Output = 0 V
		on	Output = 24 V
C2 green	Ref	off	Input = 0 V or open
		on	Input = 24 V
D2 green	N2	off	Output = 0 V
		on	Output = 24 V




Fig. 2.1.3-2: Display elements g063702x

### 2.1.3.4 Schematic Diagram



## 2.1.3.5 Technical Data

<b>Module specific Data</b>	
Sensor connection	A, /A, B, /B, C, /C (/A, /B, /C are inversed)
Current consumption (internal)	110 mA
Counter	32 bits binary
Operation Mode Capture	32 bits
Operation Mode Preload	32 bits
Quadrature decoder	4-fold interpretation
Zero impulse latch	32 bits
Commands	read, write, activate
Velocity	16 Bit (increments per 1ms)
Max. operating frequency	250 kHz
Time constant input LATCH	364 $\mu$ s
Time constant input GATE	32 $\mu$ s
Time constant input REF	32 $\mu$ s
Power supply	DC 24 V (- 15 % ... + 20 %)
Current consumption (24 V)	12 mA (without sensor and without load)
Sensor Operation voltage	DC 5 V
Sensor Output current <sub>max</sub>	300 mA
Internal bit width	1 x 32 bits data 2 x 8 bits control / status
Dimensions W x H* x L * from upper edge of DIN 35 rail	24 mm x 64 mm x 100 mm
Weight	ca. 105 g
<b>Digital Outputs (N1, N2)</b>	
Output voltage	DC 24 V
Output current <sub>max.</sub>	0,5 A short-circuit-protected
Output resistance <sub>typ.</sub>	160 m $\Omega$
<b>Digital Inputs (Latch, Gate, Ref)</b>	
Input voltage	(0) DC -3 V ... +5 V (1) DC +15 V ... +30 V
Input current <sub>typ.</sub>	Latch: 5 mA Gate and Ref: 7 mA
<b>Quadrature Inputs (A, /A, B, /B, C, /C)</b>	
Input voltage A, /A	(0) DC -30 V < (U(A) - U(/A)) < DC -15 V (1) DC +30 V > (U(A) - U(/A)) > DC +15 V
Input voltage B, /B	(0) DC -30 V < (U(B) - U(/B)) < DC -15 V (1) DC +30 V > (U(B) - U(/B)) > DC +15 V
Input voltage C, /C	(0) DC -30 V < (U(C) - U(/C)) < DC -15 V (1) DC +30 V > (U(C) - U(/C)) > DC +15 V

Standards and Regulations (cf. Chapter 2.2 of the Coupler/Controller Manual)		
EMC-Immunity to interference (CE)	acc. to EN 50082-2 (96)	
EMC-Emission of interference (CE)	acc. to EN 50081-1 (93)	
Approvals (cf. Chapter 2.2 of the Coupler/Controller Manual)		
	cUL <sub>US</sub> (UL508)	
	cUL <sub>US</sub> (UL1604)	Class I Div2 ABCD T4A
	Conformity Marking	



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### More Information

Detailed references to the approvals are listed in the document "Overview Approvals WAGO-I/O-SYSTEM 750", which You can find on the CD ROM ELECTRONICC Tools and Docs (Item-No.: 0888-0412/...) or in the Internet under:

[www.wago.com](http://www.wago.com) -> Service /Downloads /Documentation /WAGO-I/O-SYSTEM 750/System Description/.

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Further „General Technical Data“ for the WAGO-I/O-SYSTEM 750 is available in the specific fieldbus coupler / controller manuals.

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### 2.1.3.6 Functional Description

Typically, incremental encoders supply two output signals of the encoder track, both 90° offset. These signals are designated A and B. To improve the common mode interference suppression, both signals are transmitted as differential signals. In addition to the A signal, also the inverted /A level is transmitted. The difference of the input signals is evaluated in the incremental encoder I/O module. The phase position changes from A to B by changing A and /A. In this manner, it is possible to pre-define the desired counting direction by wiring.

Usually, incremental encoders have an index track in addition to the two track signals. This index track only produces one pulse per one full encoder revolution. This pulse and the counter reading can be used to determine the absolute encoder position during rotation. The index pulse has a duration of a track position pulse. We recommend to always have the latch process performed in the same rotational direction.

<b>Input</b>	<b>Function</b>
A, /A, B, /B	Quadrature input, 24 V, differential Increment pulse signal channel A or B of the Incremental Encoder
C, /C	Zero reference input, 24 V, differential Incremental encoder index pulse Dependent on the operating mode, the counter reading is taken over into the latch register or the counter showing the set value is additionally loaded, if the input edge is positive.
LATCH	LATCH input 24 V Dependent on the operating mode, the counter reading is taken into the latch register or the counter showing the set value is additionally loaded, if the input edge is positive.
GATE	GATE input, 24 V The counting process is locked if 24 V is applied to input GATE.
REF	REF input, 24 V During a reference run, the index pulse is only evaluated in conjunction with an additional sensor signal (Ref).
Screen (Shield)	Connection for the encoder line screen The screen connection is directly routed to the carrier rail.
+24V	24 V supply voltage for the module
0V	Ground for the 24 V supply voltage
<b>Output</b>	<b>Function</b>
N1, N2	Cam output, 24 V, 0.5 A "1" - Counter value is within of the defined range "0" - Counter value is outside of the defined range

### 2.1.3.7 Process Image

Using the I/O module 750-637/000-001, a 6 byte input and output process image can be transferred to the fieldbus coupler / controller via two logical channels.

The set values are stored in 4 output bytes (D0, D1, D2, D3) and the process data are stored in 4 input bytes (D0, D1, D2, D3). Two control bytes (C0, C1) and two status bytes (S0, S1) are used to select process data and set values as well as to control the data flow.



#### Attention

The representation of the process data of some I/O modules or their variations in the process image depends on the fieldbus coupler/-controller used. Please take this information as well as the particular design of the respective control/status bytes from the section "Fieldbus Specific Design of the Process Data" included in the description concerning the process image of the corresponding coupler/controller.

Input data		Output data	
S0	Status byte S0	C0	Control byte C0
D0	Process data byte 0 (LSB)	D0	Set value byte 0 (LSB)
D1	Process data byte 1	D1	Set value byte 1
S1	Status byte S1	C1	Control byte C1
D2	Process data byte 2	D2	Set value byte 2
D3	Process data byte 3 (MSB)	D3	Set value byte 3 (MSB)

Bit 0 and bit 1 in the control byte C1 determines the process data.

- Counter value
- Latch value
- Velocity
- Set value

The setting is mirrored in status byte S1 in bit 0 and bit 1.

MapPZD (Control Byte C1 / Status Byte S1, Bit 0 and 1)		
Bit 1	Bit 0	Coding of the Process data
0	0	Counter value
0	1	Latch value
1	0	Velocity (Increments per milliseconds)
1	1	Set value

Status Byte S0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	X	AckSet LoadExt	OVER- FLOW	UNDER- FLOW	CNT_ SET_ ACK	LAT_ EXT_ VAL	LATC_ VAL

LATC_ VAL	Acknowledge bit for EN_LATC (C0.0). Latch Mode: This bit is set with a positive edge at input C. It is reset when EN_LATC is reset. Preload Mode: This bit is set with a positive edge at C. It is reset when EN_LATC is reset.
LAT_ EXT_ VAL	Acknowledge bit for EN_LAT_EXT (C0.1). Latch Mode: This bit is set with a positive edge at the input Latch. It is reset when EN_LAT_EXT is reset. Preload Mode: This bit is set with a positive edge at the input Latch. It is reset when EN_LAT_EXT is reset.
CNT_ SET_ ACK	Acknowledge bit for CNT_SET (C0.2). Reset if CNT_SET=0
UNDER- FLOW	UNDERFLOW=1 with a counter overflow of 0x00000000 to 0xffffffff UNDERFLOW=0 if counter < 0xAAAAAAAA UNDERFLOW=0 if positive edge ResetUnderflow (C1.3) UNDERFLOW=0 if OVERFLOW=1
OVER- FLOW	OVERFLOW=1 with a counter overflow of 0xffffffff to 0x00000000 OVERFLOW=0 if counter > 0x55555555 OVERFLOW=0 if positive edge ResetOverflow (C1.4) OVERFLOW=0 if UNDERFLOW=1
AckSet LoadExt	Acknowledge bit for SetLoadExt. Reset if SetLoadExt=0 (C0.5)
X	reserved
0	reserved

Status Byte S1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	N2	N1	StaN2	StaN1	MapPZD	MapPZD

MapPZD	Coding of process data (2 Bits)
StaN2	State of cam output 1: 0 = cam output 1 reset, 1 = cam output 1 set
StaN1	State of cam output 2: 0 = cam output 2 reset, 1 = cam output 2 set
N1	Cam window 1st bit is set, if: bottom comparative value N1 <= Counter reading <= top comparative value N1
N2	Cam window 2nd bit is set, if: bottom comparative value N2 <= Counter reading <= top comparative value N2
0	reserved



Control Byte C1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Enable Ref	Set Nocke2	Set Nocke1	Dis Nocke2	Dis Nocke1	MapPZD	MapPZD

MapPZD Coding of Process data (2 bits)

DisNocke1 Disable cam output 1:  
0 = cam output 1 enabled, 1 = cam output 1 disabled

DisNocke2 Disable cam output 2:  
0 = cam output 2 enabled, 1 = cam output 2 disabled

SetNocke1 With a positive edge, the set value is taken over as the bottom comparative value for output 1 (N1).

With a negative edge, the set value is taken over as the top comparative value for output 1 (N1).

SetNocke2 With a positive edge, the set value is taken over as bottom comparative value for output 2 (N2).

With a negative edge, the set value is taken over as top comparative value for output 2 (N2).

EnableRef Input REF released.

- The controls set Bit EnableRef

- The controls must release EN\_LATC (C1.0) or EN\_LAT\_EXT (C1.1) with a positive edge

- A positive edge is created at input REF

- Subsequently, the next positive edge at input C or input Latch leads to a Capture or Preload event

0 reserved

## 2.1.4 750-637/000-002 [Inc.Enc./24V/32Bit/S.E.]

Incremental encoder interface 24 V / 32 bit / single ended

### 2.1.4.1 View

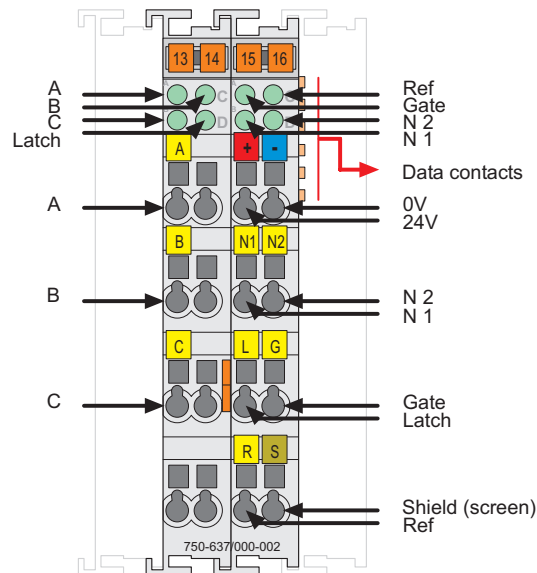


Fig. 2.1.4-1: View

g063720e

### 2.1.4.2 Description

The I/O module 750-637/000-002 represents an interface for any type of incremental encoder with an single ended 24 V connection.

The data width of the encoder module is 32 bits. Either the current counter reading, the latch value, the set value or the current speed can be mapped into the process data.

Inputs/Outputs	
A, B	Quadrature input, 24 V, single ended
C	Zero reference input, 24 V, single ended
Latch, Gate, Ref	Input, 24 V
N1, N2	Output, 24 V

A counter with quadrature decoder and a latch for the zero pulse can be read and activated by the PLC. The PLC is able to set the counter. Depending on the operating mode, the counter reading is taken into the latch register, if the edge at input "C" or "Latch" is positive.

The speed (increments/ms) is automatically recorded and can be transmitted as an alternative to the latch value.

The „Gate” input allows to lock the counter. The „Ref” input can be set to activate the zero mark „C”.

The I/O module signals whether the counter reading is within the defined set points by using the cam outputs (N1, N2). The set points can be individually set.

The I/O module requires 24 VDC power supply.

The sensor is fed with an external power supply. The sensor ground must be connected to the 0V terminal of the module.



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**Attention**

This module has no power contacts. For field supply to downstream I/O modules, a supply module will be needed.

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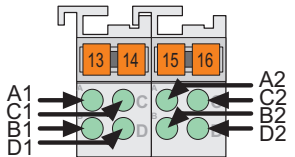
The shield (screen) is directly connected to the carrier rail.

The module 750-637/000-002 can be used with all couplers/controllers of the WAGO-I/O-SYSTEM 750 (except for the economy types 750-320, -323, -324 and -327).

This description is valid for the XXXX0301... hardware and software version. The version is specified in the manufacturing number, which is part of the lateral marking on the module.

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2.1.4.3 Display Elements



LED	Designation	Status	Function
A1 green	A	off	$0\text{ V} < U(A) < 5\text{ V}$ or input open
		on	$30\text{ V} > U(A) > 15\text{ V}$
B1 green	C	off	$0\text{ V} < U(C) < 5\text{ V}$ or input open
		on	$30\text{ V} > U(C) > 15\text{ V}$
C1 green	B	off	$0\text{ V} < U(B) < 5\text{ V}$ or input open
		on	$30\text{ V} > U(B) > 15\text{ V}$
D1 green	Latch	off	Input = 0 V or open
		on	Input = 24 V
A2 green	Gate	off	Input = 0 V or open
		on	Input = 24 V
B2 green	N1	off	Output = 0 V
		on	Output = 24 V
C2 green	Ref	off	Input = 0 V or open
		on	Input = 24 V
D2 green	N2	off	Output = 0 V
		on	Output = 24 V

Fig. 2.1.4-2: Display elements g063702x

2.1.4.4 Schematic Diagram

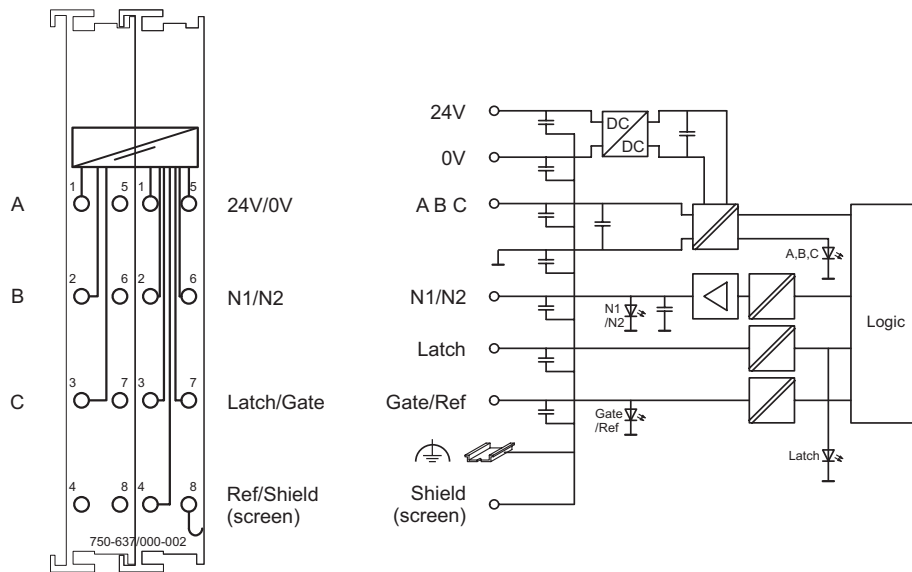





Fig. 2.1.4-2: Schematic Diagram

## 2.1.4.5 Technical Data

<b>Module specific Data</b>	
Sensor connection	A, B, C, 0 V
Current consumption (internal)	110 mA
Counter	32 bits binary
Operation Mode Capture	32 bits
Operation Mode Preload	32 bits
Quadrature decoder	4-fold report
Zero impulse latch	32 bits
Commands	read, write, activate
Velocity	16 Bit (Increments per 1ms)
Max. operating frequency	250 kHz
Time constant input LATCH	364 $\mu$ s
Time constant input GATE	32 $\mu$ s
Time constant input REF	32 $\mu$ s
Power supply	DC 24 V (- 15 % ... + 20 %)
Current consumption (24 V)	12 mA (without sensor and without load)
Sensor Operation voltage	DC 5 V
Sensor Output current $_{max}$	300 mA
Internal bit width	1 x 32 bits data 2 x 8 bits control/status
Dimensions W x H* x L * from upper edge of DIN 35 rail	24 mm x 64 mm x 100 mm
Weight	ca. 105 g
<b>Digital Outputs (N1, N2)</b>	
Output voltage	DC 24 V
Output current $_{max.}$	0,5 A short-circuit-protected
Output resistance $_{typ.}$	160 m $\Omega$
<b>Digital Inputs (Latch, Gate, Ref)</b>	
Input voltage	(0) DC -3 V ... +5 V (1) DC +15 V ... +30 V
Input current $_{typ.}$	Latch: 5 mA Gate and Ref: 7 mA
<b>Quadrature Inputs (A, /A, B, /B, C, /C)</b>	
Input voltage A, /A	(0) DC 0 V < U(A) < DC 5 V (1) DC 30 V > U(A) > DC 15 V
Input voltage B, /B	(0) DC 0 V < U(B) < DC 5 V (1) DC 30 V > U(B) > DC 15 V
Input voltage C, /C	(0) DC 0 V < U(C) < DC 5 V (1) DC 30 V > U(B) > DC 15 V

<b>Standards and Regulations (cf. Chapter 2.2 of the Coupler/Controller Manual)</b>		
EMC-Immunity to interference (CE)	acc. to EN 50082-2 (96)	
EMC-Emission of interference (CE)	acc. to EN 50081-1 (93)	
<b>Approvals (cf. Chapter 2.2 of the Coupler/Controller Manual)</b>		
	cUL <sub>US</sub> (UL508)	
	cUL <sub>US</sub> (UL1604)	Class I Div2 ABCD T4A
	Conformity Marking	




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**More Information**

Detailed references to the approvals are listed in the document "Overview Approvals WAGO-I/O-SYSTEM 750", which You can find on the CD ROM ELECTRONICC Tools and Docs (Item-No.: 0888-0412/...) or in the Internet under:

[www.wago.com](http://www.wago.com) -> Service /Downloads /Documentation /WAGO-I/O-SYSTEM 750/System Description/.

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Further „General Technical Data“ for the WAGO-I/O-SYSTEM 750 is available in the specific fieldbus coupler / controller manuals.

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### 2.1.4.6 Functional Description

Typically, incremental encoders supply two output signals of the encoder track, both 90° offset. These signals are designated A and B. The difference of the input signals is evaluated in the incremental encoder I/O module.

Usually, incremental encoders have an index track in addition to the two track signals. This index track only produces one pulse per one full encoder revolution. This pulse and the counter reading can be used to determine the absolute encoder position during rotation. The index pulse has a duration of a track position pulse. We recommend to always have the latch process performed in the same rotational direction.

<b>Input</b>	<b>Function</b>
A, B	Quadrature input, 24 V, single ended Increment pulse signal channel A or B of the Incremental Encoder
C	Zero reference input, 24 V, single ended Incremental encoder index pulse Dependent on the operating mode, the counter reading is taken over into the latch register or the counter showing the set value is additionally loaded, if the input edge is positive.
LATCH	LATCH input 24 V Dependent on the operating mode, the counter reading is taken into the latch register or the counter showing the set value is additionally loaded, if the input edge is positive.
GATE	GATE input, 24 V The counting process is locked if 24 V is applied to input GATE.
REF	REF input, 24 V During a reference run, the index pulse is only evaluated in conjunction with an additional sensor signal (Ref).
Screen (Shield)	Connection for the encoder line screen The screen connection is directly routed to the carrier rail.
+24V	24 V supply voltage for the module
0V	Ground for the 24 V supply voltage
<b>Output</b>	<b>Function</b>
N1, N2	Cam output, 24 V, 0.5 A "1" - Counter value is within of the defined range "0" - Counter value is outside of the defined range

### 2.1.4.7 Process Image

Using the I/O module 750-637/000-002, a 6 byte input and output process image can be transferred to the fieldbus coupler / controller via two logical channels.

The set values are stored in 4 output bytes (D0, D1, D2, D3) and the process data are stored in 4 input bytes (D0, D1, D2, D3). Two control bytes (C0, C1) and two status bytes (S0, S1) are used to select process data and set values as well as to control the data flow.



#### Attention

The representation of the process data of some I/O modules or their variations in the process image depends on the fieldbus coupler/-controller used. Please take this information as well as the particular design of the respective control/status bytes from the section "Fieldbus Specific Design of the Process Data" included in the description concerning the process image of the corresponding coupler/controller.

Input data		Output data	
S0	Status byte S0	C0	Control byte C0
D0	Process data byte 0 (LSB)	D0	Set value byte 0 (LSB)
D1	Process data byte 1	D1	Set value byte 1
S1	Status byte S1	C1	Control byte C1
D2	Process data byte 2	D2	Set value byte 2
D3	Process data byte 3 (MSB)	D3	Set value byte 3 (MSB)

Bit 0 and bit 1 in the control byte C1 determines the process data.

- Counter value
- Latch value
- Velocity
- Set value

The setting is mirrored in status byte S1 in bit 0 and bit 1.

MapPZD (Control Byte C1 / Status Byte S1, Bit 0 and 1)		
Bit 1	Bit 0	Coding of the Process data
0	0	Counter value
0	1	Latch value
1	0	Velocity (Increments per milliseconds)
1	1	Set value

Status Byte S0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	X	AckSet LoadExt	OVER- FLOW	UNDER- FLOW	CNT_ SET_ ACK	LAT_ EXT_ VAL	LATC_ VAL

LATC_ VAL	Acknowledge bit for EN_LATC (C0.0). Latch Mode: This bit is set with a positive edge at input C. It is reset when EN_LATC is reset. Preload Mode: This bit is set with a positive edge at C. It is reset when EN_LATC is reset.
LAT_ EXT_ VAL	Acknowledge bit for EN_LAT_EXT (C0.1). Latch Mode: This bit is set with a positive edge at the input Latch. It is reset when EN_LAT_EXT is reset. Preload Mode: This bit is set with a positive edge at the input Latch. It is reset when EN_LAT_EXT is reset.
CNT_ SET_ ACK	Acknowledge bit for CNT_SET (C0.2). Reset if CNT_SET=0
UNDER- FLOW	UNDERFLOW=1 with a counter overflow of 0x00000000 to 0xffffffff UNDERFLOW=0 if counter < 0xAAAAAAAA UNDERFLOW=0 if positive edge ResetUnderflow (C1.3) UNDERFLOW=0 if OVERFLOW=1
OVER- FLOW	OVERFLOW=1 with a counter overflow of 0xffffffff to 0x00000000 OVERFLOW=0 if counter > 0x55555555 OVERFLOW=0 if positive edge ResetOverflow (C1.4) OVERFLOW=0 if UNDERFLOW=1
AckSet LoadExt	Acknowledge bit for SetLoadExt. Reset if SetLoadExt=0 (C0.5)
X	reserved
0	reserved

Status Byte S1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	N2	N1	StaN2	StaN1	MapPZD	MapPZD

MapPZD	Coding of process data (2 Bits)
StaN2	State of cam output 1: 0 = cam output 1 reset, 1 = cam output 1 set
StaN1	State of cam output 2: 0 = cam output 2 reset, 1 = cam output 2 set
N1	Cam window 1st bit is set, if: bottom comparative value N1 <= Counter reading <= top comparative value N1
N2	Cam window 2nd bit is set, if: bottom comparative value N2 <= Counter reading <= top comparative value N2
0	reserved



Control Byte C1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Enable Ref	Set Nocke2	Set Nocke1	Dis Nocke2	Dis Nocke1	MapPZD	MapPZD

MapPZD Coding of Process data (2 bits)

DisNocke1 Disable cam output 1:  
0 = cam output 1 enabled, 1 = cam output 1 disabled

DisNocke2 Disable cam output 2:  
0 = cam output 2 enabled, 1 = cam output 2 disabled

SetNocke1 With a positive edge, the set value is taken over as the bottom comparative value for output 1 (N1).

With a negative edge, the set value is taken over as the top comparative value for output 1 (N1).

SetNocke2 With a positive edge, the set value is taken over as bottom comparative value for output 2 (N2).

With a negative edge, the set value is taken over as top comparative value for output 2 (N2).

EnableRef Input REF released.

- The controls set Bit EnableRef

- The controls must release EN\_LATC (C1.0) or EN\_LAT\_EXT (C1.1) with a positive edge

- A positive edge is created at input REF

- Subsequently, the next positive edge at input C or input Latch leads to a Capture or Preload event

0 reserved



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